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Deep-Learning Based Depth-Tracking of Stacking-Faults in Epitaxially Grown Silicon Wafers

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Abstract. Stacking faults in epitaxial silicon wafers are structural defects that can reduce the recombination lifetime of the final solar cells significantly. They are known to originate mostly at the interface between substrate and deposited layer, at contamination particles and atomic steps. This work presents a non-destructive and automated characterization method on full-size wafers to locate stacking faults and determine their layer of origin to identify process-based root causes. A deep learning model and a quantification via geometric defect properties is realized on dark field microscope images, with the potential to be transferred to inline images measured in dark field mode with high-resolution cameras. We achieve detection rates up to 92% for regular wafer surfaces. The depth analysis combines geometric properties of the stacking faults and measured wafer thickness and is applied on full-scale epitaxial wafers. Most stacking faults are confirmed to originate at the interface layer and their number is higher by 1-2 orders of magnitude when deposition occurs on a reorganized porous layer. However, our results also indicate that a non-negligible part of stacking faults has its origin within the epitaxial layer.

Keywords: Kerfless Silicon Growth, Stacking Faults, Image Segmentation, Quality Inspection

1. Introduction

Kerf-less wafer technologies are advantageous in terms of material cost and reduced energy consumption. With the objective of a large-scale production that can compete with Czochralski growth of silicon, it is crucial to minimize lifetime-decreasing defects like stacking faults. While the characterization of stacking faults and their origin on microscopic scale has already been research topic of phenomenological studies [1-3], in this contribution, the focus is on a full wafer characterization that can be integrated into the industrial process.

Our method enables a fully automated detection of 3D stacking fault positions in highly resolved microscope images. Their lateral position on the wafer is identified by a segmentation with a deep-learning model. The third dimension is the depth of the stacking fault origin. It is tracked down virtually by making use of their pyramidal geometry: the (111) planes build an inverted pyramidal structure, see Figure 1. Combined with thickness measurements before and after epitaxial growth, such an information can assist in defining the layer where the stacking fault originated. Accordingly, the growth of stacking faults can be mitigated by addressing the process-related challenges at the respective stage.

2. Experimental and Algorithmic Approach

2.1 Experimental Approach

The measurements applied for this experiment are shown in Figure 1, along with a schematic view of the layers in epitaxially grown silicon. The epitaxial wafers were measured via dark field microscopy (resolution 1.7 µm/px). An image of the whole wafer (size 156.7 mm x 156.7 mm) is obtained by stitching 47 x 77 single rectangular images. The thickness of the substrate was measured via triangulation on three traces of an inline wafer inspection system with a resolution of ~180 µm/px. The thickness of the wafer after epitaxy was measured in an offline tool with a spatial resolution of ~2 mm/px. The thickness data were interpolated (linearly) to match with the microscope data. To account for the low resolution, we added a tolerance to the interface thickness, which is usually between 1 and 2 µm, of which we assumed the upper bound 2 µm. This tolerance amounts to sum of the individual substrate thickness variation of the wafer (median 18.2 µm) and the combined uncertainty of the thickness measurements of 1.14 µm.

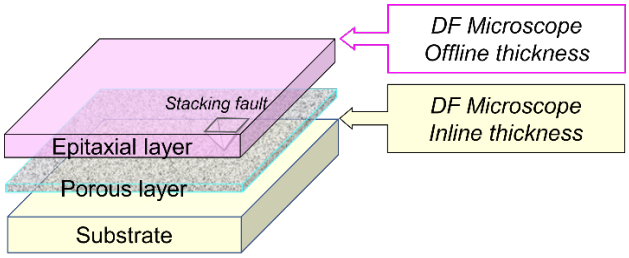

Figure 1. *Schematic view on the layers of an epitaxially grown silicon wafer. The boxes denote the measurements serving as basis for our analysis: dark Field (DF) microscopy and thickness measurements.*

2.2 Algorithmic Approach

As outlined in Figure 2 b), the algorithmic approach is split into two steps:

Step 1: Training and application of models for stacking fault recognition: To achieve a semantic segmentation of stacking faults, a U-Net [4] has been trained on 243 annotated single microscope images. The dataset is split 80%/20% into training and validation set. Two classes of stacking faults are discerned: so-called “open” and “closed” stacking faults that are flattened pyramids, with a level only slightly elevated above the surface. They appear as squares with bright outlines. The second consists in full pyramids that appear as filled bright squares. With basic image processing, the labeled dataset was extended to be applicable to a more varied dataset. It includes wafers grown with different process sequences and process configurations on different substrate materials and thus represents a broad variety of stacking fault density and appearance. Preprocessing and augmentation involve an alignment and scaling, rotations and further transforms regarding blurring and noise. By an inference of these models, a semantic segmentation of stacking faults is obtained. Stacking faults with only one visible side were labeled but not used for this analysis of depth calculation since the determination of the length of a single line, combined with noisy data, leads to high uncertainty.

Step 2: Geometric evaluation and determination of origin layer: To determine stacking fault size, template matching with binned sizes (between 130 - 300 µm) was applied on the segmentation results of Step 1. The best response yields the matched size. Figure 2 a) schematically shows how this relates to the depth of the stacking fault d_{SF}:

$$d_{\mathrm{SF}} = \frac{a}{\sqrt{2}} = \tan(\alpha')\frac{a}{2}, \text{ with } \alpha = 45°,\ \alpha' = \tan^{-1}\sqrt{2} \approx 54.7°. \quad (1)$$

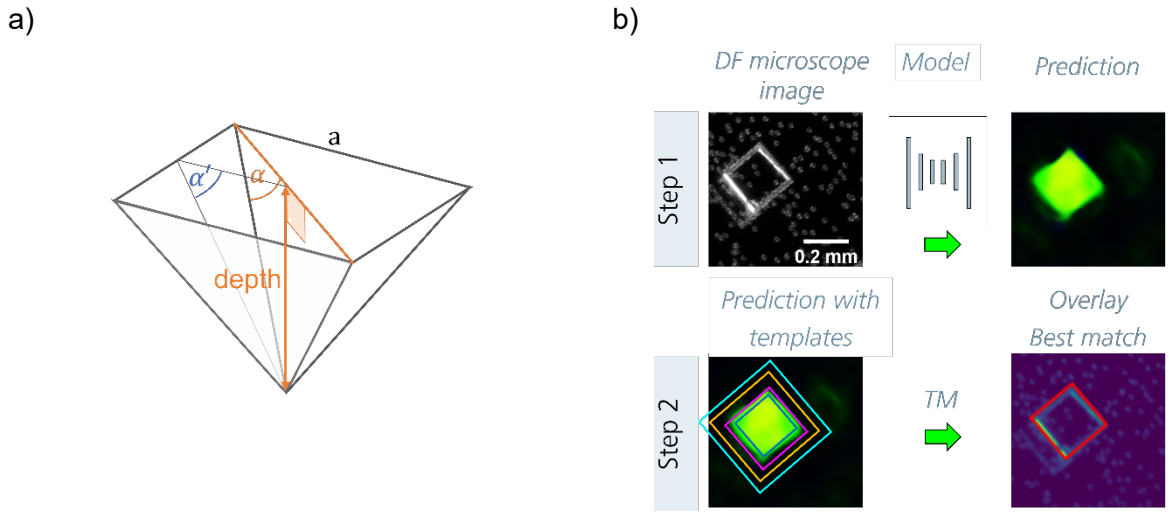

***Figure 2**. Left: Schematic view on a stacking fault grown as inverted pyramid. Right: Algorithmic approach. Top, step 1: Dark-field microscope image (image section) and segmentation result (same image section) obtained with a deep learning model. Bottom, Step 2: Template matching with binned template sizes and best match.*

A confidence measure is computed based on the ideal match and used as a criterion to remove false positives a posteriori. By subtracting the determined depth with the thickness of the epitaxial layer $d_{\mathrm{Epi}}, d_L = d_{Epi} - d_{SF}$, the origin is assigned to one of three classes according to the sign of $d_{\mathrm{SF}} </=/> d_{\mathrm{Epi}}$, i.e., originated in the substrate (<), at the interface (=) or within the epitaxial layer (>). Since our experiment was carried out before detachment, d_{Epi} is determined by subtracting the substrate thickness from the overall thickness: $d_{\mathrm{Epi}} = d_{\mathrm{Wafer}} - d_{\mathrm{Substrate}}$.

3. Results

In Figure 3, results for different cases of detection and size matching are shown. Case A accounts for at least 50% of observed stacking faults, namely separately occurring open stacking faults. The model performs well and robustly for this case. Size detection works well, slightly tending to over-estimation. Regarding successful detection, case C is similar to case A but regards closed stacking faults, which occur more rarely. They are labeled and successfully discerned as another defect class but treated in the same way for size detection. Case B shows different aspects of overlapping stacking faults that occur less frequently. Both, identification model and size detection, display restrictions in this case, the first in detecting only the more distinct stacking faults, the second in discarding non-square segmentation outputs.

3.1 Detection of stacking faults

On flat surfaces without disturbing structures, single stacking faults show a high accuracy of up to 92% for the microscope images. The used metric for accuracy is the *intersection over union,* short *IoU* with regard to pixels in labeled regions and thresholded prediction. In Figure 3, exemplary image sections of microscope images show successful detections and restrictions. Case A (first and second column) represents the most common case of stacking fault appearance for which the detection works reliably.

The detection quality is found to depend strongly on the following criteria. First, the thickness variation of the wafer. In sloped regions of the wafer surface, stacking faults often appear incomplete in the measurement. While the model is mostly able to detect partially visible stacking faults, the probability of false positives or wrong size matchings is increased with the amount of missing information about the geometry. Second, the presence of contaminations that decorate stacking faults. While the moSiliconPV Conf Proc 2 (2024) "SiliconPV 2024,

14th International Conference on Crystalline Silicon Photovoltaics"del is trained to work in those cases, the dotted surface appearance also decreases accuracy, as shown in Figure 3 case A, third example. With sloping surface and contaminations present, the IoU drops to about 60%. And third, overlapping structures, in which the detection of single stacking faults becomes ambiguous, and the size may be mismatched or discarded, see Figure 3 case B.

3.2 Layer of stacking fault origin

Regarding the overall occurrence of stacking faults, wafers from groups that underwent a porosification and reorganization show multiples of stacking faults compared to a reference without porous interface layer. For all wafers, the depth origin of the detected stacking faults was mostly near the interface between substrate and deposited layer. Additionally, a minor number of origins are indicated within the epitaxial layer.

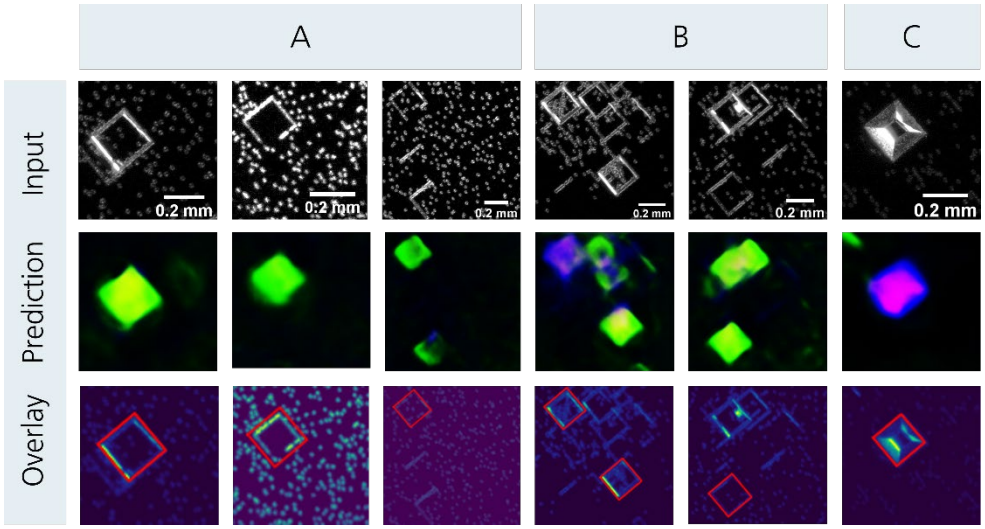

Figure 3. *Image matrix showing image sections from original microscope images (top row), segmentation results (middle row) and the best match resulting from template matching, shown as red bounding boxes. A, B and C stand for different types of stacking fault occurrence and appearance: (A) separate open stacking faults (>50%), (B) regions with overlapping stacking faults and (C) closed stacking faults.*

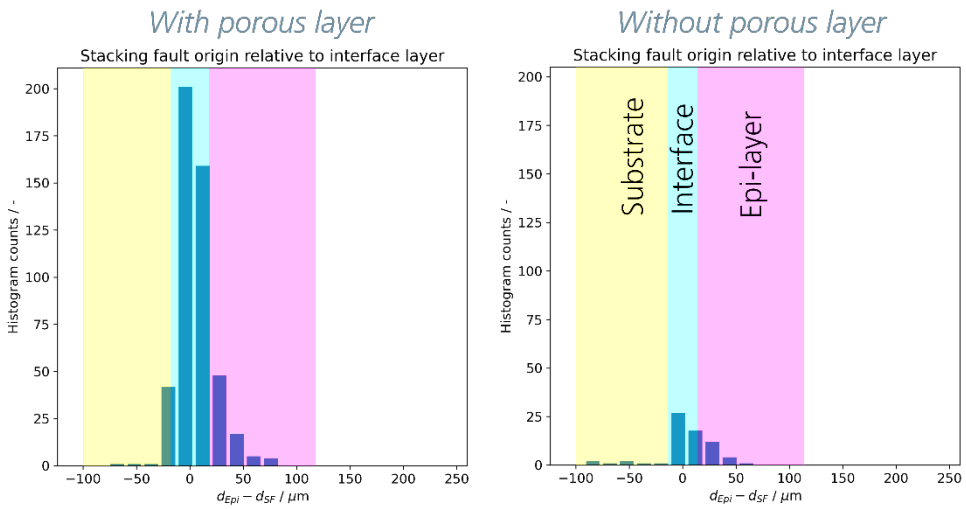

Figure 4. *Histograms showing the origin layer of detected stacking faults as determined from stacking fault depth, following our algorithmic steps, and adjusting the depth with wafer thickness measurements. The total thickness variation of the substrate is added as tolerance to the interface layer.*

4. Discussion

4.1 Suitability of the algorithmic approach

The exemplary image sections in Figure 3 show that the appearance of stacking faults can vary according to the wafer surface and presence of contaminations. Not all sides of the stacking faults are always visible. From the visual results, we can conclude that the segmentation results are indeed robust regarding those variations. In the case of overlapping regions, the recall is reduced, yet the algorithmic results still indicate a locally increased stacking fault density within those regions, and the depth information is valid regardless. In this work, stacking faults are left out of which only one side is visible. Those would have to be considered to assess material quality, yet for a reliable size determination, one line is too error prone. That means that in our results, the total number of stacking faults is underestimated.

Regarding the reliability of the determined layer of origin, the adjustment with wafer thickness measurements introduces uncertainties, first from the measurements (~1 µm) and second from using only three lines of inline thickness measurements on the substrate. We account for this by adding a tolerance of the measurement uncertainty plus the total thickness variation of the specific substrate (median 18.2 µm) as a tolerance in the depth dimension.

4.2 Probable root causes for stacking fault origins

With regard to the layer of origin in the use-cases, the results confirm the finding that most stacking faults originate between substrate and deposited layer, mostly at the reorganized porous layer, e.g. via incompletely closed pores or stress and resulting dislocations [2]. Yet, our results suggest that new stacking faults have formed within the epitaxial layer. Origins of stacking faults can be induced by contaminations, stress in general (causing dislocations) and the formation of twinned grains at atomic steps that could lead to the formation of new stacking faults [5]. Such origins of formation can occur at the growth front during epitaxial growth.

5. Conclusions and outlook

In this work, we present a non-destructive and fully automated characterization method to detect the position and layer origin of stacking faults on full-size wafers grown with an epitaxial process. The position of the stacking faults is identified based on dark-field microscope images and a convolutional neural network. Their depth is derived from the stacking fault size via the well-known geometry of these defects. Combined with wafer thickness measurements, the layer of origin can be determined. The model obtained with deep learning successfully detects most of the stacking faults and the detected size is in accordance with visual appearance except for regions with larger image noise or higher thickness variation. Our method works reliably, especially for samples with homogeneous surface. The relatively large tolerance regarding the interface depth is a restriction to our method that must be addressed in the future, for example by a characterization on detached wafers.

The model was applied on images of full wafers (with a side length of 156.7 mm), corresponding to more than 3000 single dark field microscope images per wafer with a resolution of 1.7 µm / px. The main layer of stacking fault origins is confirmed to be the interface, i.e., the layer on which the deposition takes place. The number of stacking faults is significantly lower if the deposition takes place on the substrate, compared to a reorganized porous layer. This can be attributed to agglomerated vacancies and increased stress and resulting dislocations. At the same time, our results strongly suggest further origins within the epitaxial layer. A transfer of the method to inline wafer measurements can provide an extended dataset for further investigations on new data obtained on samples from a novel industrial process.

Data availability statement

The data and code underlying our results cannot be published as part of a confidentiality agreement with a third party.

Underlying and related material

The training code of U-Net for this work was written by Siddharth Raghavendran, based on the paper by Ronneberger et al. [4], doi: 10.1007/978-3-319-24574-4_28. The remaining parts of the coding also originate from the authors, based on established image processing methods.

Author contributions

Theresa Trötschler and Matthias Demant: Conceptualization. Theresa Trötschler and Siddharth Raghavendran: Software, Data curation, Formal analysis, Investigation, Validation. Saed Al-Hajjawi: Data curation, Investigation. Theresa Trötschler: Writing, Original draft preparation, Visualization. Matthias Demant: Supervision (analytic part) Jonas Haunschild: Supervision (experimental part). Matthias Demant and Stefan Rein: Reviewing and Editing,

Competing interests

The authors declare that they have no competing interests.

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