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Investigation of the Impact of the Wafer Resistivities on Double-Side Passivated Contact Silicon Solar Cells

Pradeep Padhamnath[1], Gabby De Luna[1], Ruohan Zhong[2], John Derek Arcebal[1], Ajeet Rohatgi[2], and Armin G. Aberle[1]

[1] Solar Energy Research Institute of Singapore, National University of Singapore, Singapore

[2] Georgia Institute of Technology, USA

*Correspondence: Pradeep Padhamnath, pradeep.p@u.nus.edu

Abstract. In this work, we investigate the impact of substrate resistivities on the performance of poly-Si based double-side passivated contact solar cells, featuring high-temperature fire-through contacts to both n-type and p-type poly-Si, where the contacts are co-fired at the same firing temperatures. Large-area double-side passivated contact solar cells are fabricated on n-type wafers and thoroughly characterized to understand the impact of the change in Si wafer resistivity on the performance of the solar cells. The solar cells are fabricated on n-type substrates, with p^+ poly-Si deposited on the planar rear side and n^+ poly-Si on the textured front. The n^+ poly-Si on the front side is selectively patterned to constrain it to the regions below the metal contacts. The fabricated solar cells achieve ≈ 22% efficiency on large area using high-temperature fire-through metallization. With the help of detailed characterization, we identify the losses that limit the device efficiency.

Keywords: Passivated Contacts, Polysilicon, Screen Printing, Selective Contact, Inkjet

1. Introduction

Silicon solar cells incorporating passivating contacts based on doped polysilicon (poly-Si) are being ramped up quickly in the PV industry and are poised to replace PERC as the dominant solar cell in the world markets [1]. Passivated contact solar cells now exceeded efficiencies of 24% in commercial production [2]. The combination of iO_x/doped poly-Si layers provide excellent passivation and contact properties. Nevertheless, the parasitic absorption in the poly-Si layers have predominantly limited the application of the technology to the rear surface of the solar cells [3].

However, there has been recent increased interest in incorporating the poly-Si based passivating contacts on both the front and rear side of the solar cells (DS-TOPCon). Recently efficiencies exceeding 22% have been reported for such solar cells fabricated on large-area (≈ 244 cm^2) n-type substrates [4], [5]. Several methods have been reported for fabrication of such solar cells. A low-temperature metallization process such as plating or thermal evaporation of the contacts could be used to minimize damage to the front poly-Si layers, which are kept thin to limit the parasitic absorption [6], [7]. In another approach the poly-Si layer on the front was limited only under the metal contacts [8]. Limiting the front poly-Si layers to only under the metal contacts helps in achieving excellent contact passivation while minimizing the losses in the short-circuit current density (J_{sc}) due to the absorption in the poly-Si layer. In recent works,

such solar cells were reported where the poly-Si on the front was patterned using an industrial inkjet process. The metal contacts to the poly-Si layers on both sides were screen-printed using high-temperature fire-through (FT) pastes reaching cell efficiencies of 22% [4]. A similar approach used with nFT Al pastes reached efficiencies of 22.5% [5]. Such solar cells have the potential to exceed 26% efficiency due to the reduced recombination and good contact passivation on the front side [4], [9]. These solar cells are also suitable for use as bottom cells in perovskite-silicon tandem solar cells [10].

In this work, we investigate the impact of substrate resistivities on the performance of poly-Si based double-side passivated contact solar cells, featuring high-temperature fire-through contacts to both phosphorus (P) doped (n^+) and boron (B) doped (p^+) poly-Si layers. Both contacts are co-fired at the same firing temperatures, which reduces the complexity in the fabrication process. Large-area rear-junction double-side passivated contact solar cells are fabricated on n-type wafers. The process is thoroughly characterized with the help of several test samples. The solar cells are characterized and analysed to understand the impact of the change in Si wafer resistivity on the performance of the devices. The solar cells are fabricated on n-type substrates, with p^+ poly-Si deposited on planar rear side and n^+ poly-Si on the textured front, resulting in a rear-junction configuration. The n^+ poly-Si on the front side is selectively patterned so as to constrain it to the regions below the metal contacts. The fabricated solar cells achieve ≈ 22% efficiency. With the help of detailed characterization, we identify the losses that limit the device efficiency.

2. Experimental Details

Samples and solar cells are fabricated on large-area (M2, 15.6 x 15.6 cm^2) n-type wafers. The wafers were grouped into three sets of different resistivities (1.0, 1.5, 1.8 Ω-cm). Some p-type test wafers were also used to prepare the test samples. Test samples are either symmetrically polished in KOH (20%) or symmetrically textured in KOH (2%) solution. 250 nm of intrinsic poly-Si is deposited on the rear side while 100 nm of intrinsic poly-Si is deposited on the front using the Low-Pressure Chemical Vapour Deposition (LPCVD) process. The rear poly-Si was doped with boron using boron tribromide (BBr_3) as the dopant source, while the front poly-Si was doped with phosphorus using phosphorus oxychloride ($POCl_3$) as the dopant source in a high-temperature furnace. The polysilicon on the front side is patterned using an industrial inkjet printer [SuSS IP410] to limit it to the regions below the metal contacts. The patterned poly-Si on the front is referred to as ‘poly-Si fingers’ while the area where the poly-Si was etched is referred to as the ‘wing region’. The details of the patterning can be found in the literature [4], [5]. The polysilicon regions under the metal contacts are referred to as ‘fingers’ while the area between the poly-Si fingers is referred to as the ‘field’ region. Contacts are formed with commercially available Ag pastes (to n-type poly-Si) and Ag-Al pastes (to p-type poly-Si) using screen-printing and fired at high temperature. Further, characterization of the solar cells and loss analysis is carried out.

The sheet resistance of the doped poly-Si layers was mapped on the whole area using a four-point probe tool. The active dopant concentration was charted using an electrochemical capacitance measurement tool. The passivation quality of the doped poly-Si/iO_x passivated contact layer was determined using Quasi-Steady-State Photoconductance (QSSPC) measurements. QSSPC measurements were used to ascertain the implied open-circuit voltage (iV_{oc}), the saturation current density under the passivated regions ($J_{0,surf}$), the recombination current density in the bulk region ($J_{0,bulk}$) and the implied fill factor (iFF). The external quantum efficiency (EQE) and reflectance of the solar cells were analysed using the spot EQE and reflectance measurement system, using an integrating sphere. The specific contact resistivity (ρ_c) was measured using the modified transfer length measurement (TLM) method and the saturation current density under the metal contacts ($J_{0,metal}$) was evaluated using photoluminescence (PL) images as explained in a previous work [11]. A cross-sectional schematic of the solar cell is shown in Figure 1.

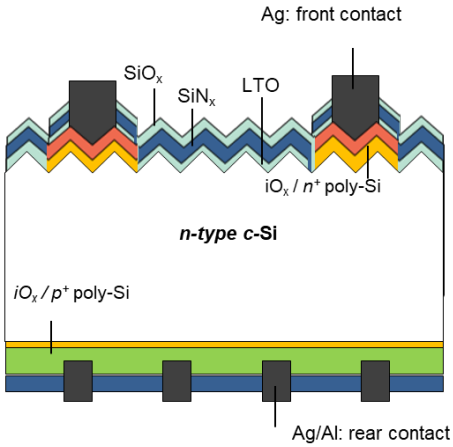

Figure 1. *Schematic of a double-side passivated contact solar cell with selective poly-Si under the front metal contacts.*

3. Experimental results and Discussion

3.1 Electrical properties of the doped poly-Si layers

Figure 2 shows the active dopant concentration of the doped poly-Si layers, as evaluated using Electrochemical Capacitance Voltage (ECV) measurements. Test wafers having opposite polarity to the dopant were used for the characterization of the electrical properties. The diffusion process is carefully optimised to achieve a high dopant concentration in the poly-Si layers, which drops off after the poly-Si layer. This is also used as an indirect measurement of the poly-Si thickness [12], [13]. The thickness of the n^+ poly-Si layers on the front textured surface was observed to be ≈ 95 nm, while the thickness of the p^+ poly-Si was estimated to be 250 nm. The peak concentration of P in the n^+ poly-Si layer reached ≈ $3x10^{20}$ cm^{-3}, while that of B in the p^+ poly-Si layer was observed to be around $7x10^{19}$ cm^{-3}. The dopant profile was also checked after patterning and etching the n^+ poly-Si layer using specially fabricated samples as described in [4], [5].

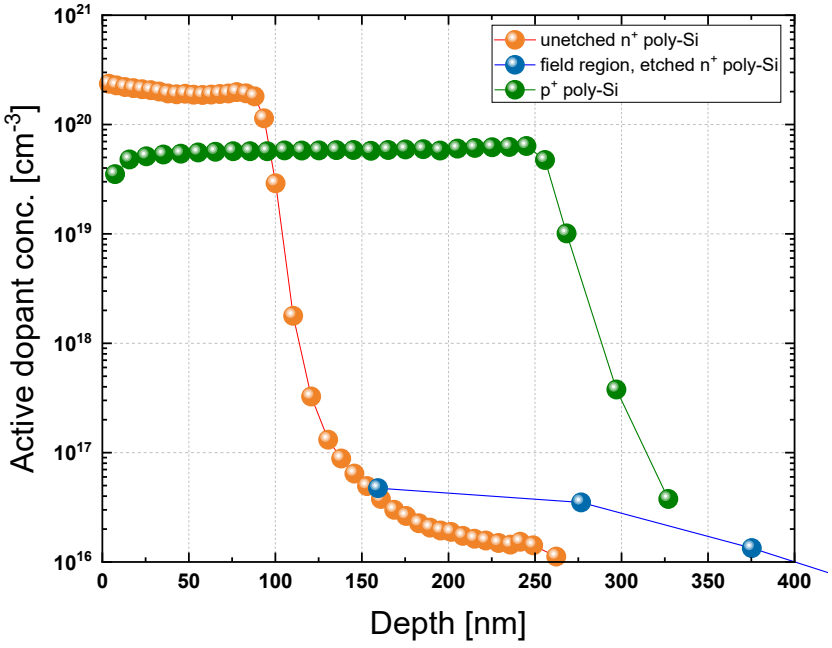

Figure 2. *ECV profiles for 100 nm n^+ poly-Si (on-p-type textured wafer), 250 nm p^+ poly-Si (on n-type planar wafer) and the textured c-Si surface after etching the n^+ poly-Si layer.*

The dopant profile after etching the n^+ poly-Si layers is also shown in Fig 2. It can be seen that the entire poly-Si layer was removed. Some doped c-Si layer containing the 'tail-end' of the diffusion profile was also removed. The data obtained from this measurement was later used as an input to the model of the solar cell.

Figure 3 shows the sheet resistance (R_{sheet}) map of the doped poly-Si layers and the region after etching the n^+ poly-Si on the test sample. The R_{sheet} of the p^+ poly-Si layer was measured to be 150 ± 2 Ω/square, while that of n^+ poly-Si was found to be 106 ± 5 Ω/square. The R_{sheet} of the etched regions was measured to be 58 ± 2 Ω/square. The difference in the R_{sheet} and the dopant concentration signify that the poly-Si layer was completely etched. This is important to avoid any parasitic absorption from the residual poly-Si layer [3], [14].

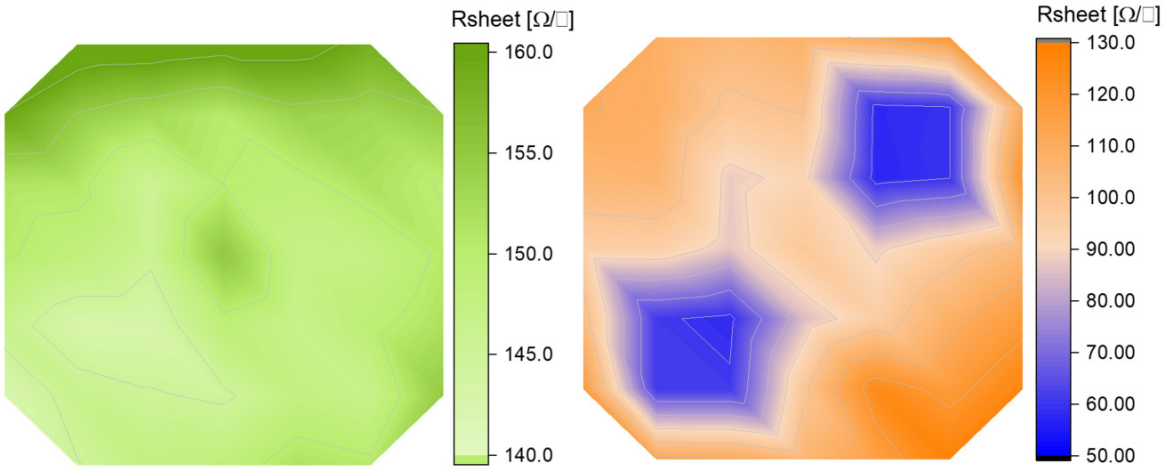

Figure 3. *R_{sheet} for 250 nm thick p^+ poly-Si on planar surface (left image), 100 nm n^+ poly-Si on textured surface and the regions where the n^+ poly-Si was chemically etched (right image).*

3.2 Passivation properties of the different solar cell surfaces

The passivation properties of the doped poly-Si layers and the etched regions were evaluated using the QSSPC measurements after depositing the antireflection coating and again after simulated firing in a high-temperature metallization furnace, using a firing profile similar to the one used for formation of metal contacts. Test samples were fabricated using the wafers with three different resistivities to ascertain its impact on the passivation performance, if any. The data obtained from QSSPC measurements for 100-nm n^+ poly-Si symmetric samples fabricated on test wafers with different resistivities are shown in Figure 4. The iV_{oc} of the samples with n^+ poly-Si layers were in the range of 710 - 720 mV for samples with different wafer resistivities. The iV_{oc} showed a slight decrease in the test samples with increasing wafer resistivity. The best iV_{oc} for 1 Ω-cm test samples was ≈ 720 mV, while the same for 1.8 Ω-cm test samples was observed to be only 710 mV. The iFF data also did not show any trends with the changing wafer resistivities and the data were similar for the samples with different resistivities.

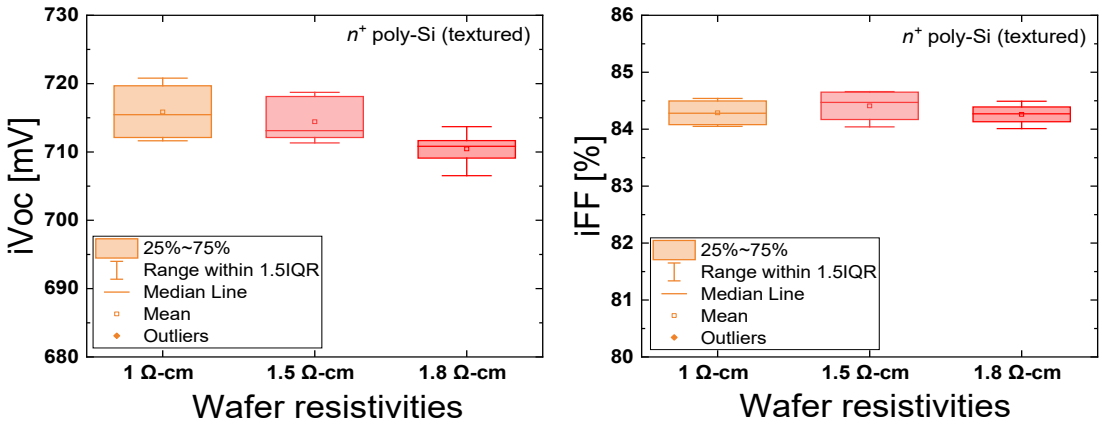

Figure 4. *QSSPC-derived properties of 100 nm n⁺ poly-Si layers on symmetrical textured test samples. a) iV_{oc}, b) iFF.*

Figure 5 shows the passivation performance of the p⁺ poly-Si layers deposited on planar surface of wafers with different resistivities. The iV_{oc} of the p⁺ poly-Si layers on planar surfaces were similar to that of n⁺ poly-Si layers on textured surface, ranging from 705-720 mV for wafers with different resistivities. The iFF values of the symmetric samples with p⁺ poly-Si were observed to be slightly lower (1-1.5% absolute) than in those with n⁺ poly-Si. Similar observations were reported earlier where the passivation properties of p⁺ poly-Si layers were observed to be slightly inferior to n⁺ poly-Si layers [13], [15]. While, unlike the samples with n⁺ poly-Si, the iV_{oc} did not show a diminishing trend with increasing wafer resistivity, the wafers with highest resistivities still resulted in the lowest iV_{oc} values, which was also observed in n⁺ poly-Si test samples (Figure 4). For p⁺ poly-Si test samples, the best iV_{oc} values (≈ 722 mV) were achieved on 1.5 Ω-cm test samples, while for the 1.8 Ω-cm test samples the maximum iV_{oc} was only 710 mV. The reason for this change in iV_{oc} could depend on the surface as well as bulk properties of the wafer. Since all wafers were processed together in the wet chemical cleaning process, it is inferred that the wafers with different resistivities may respond differently to the same chemical cleaning process.

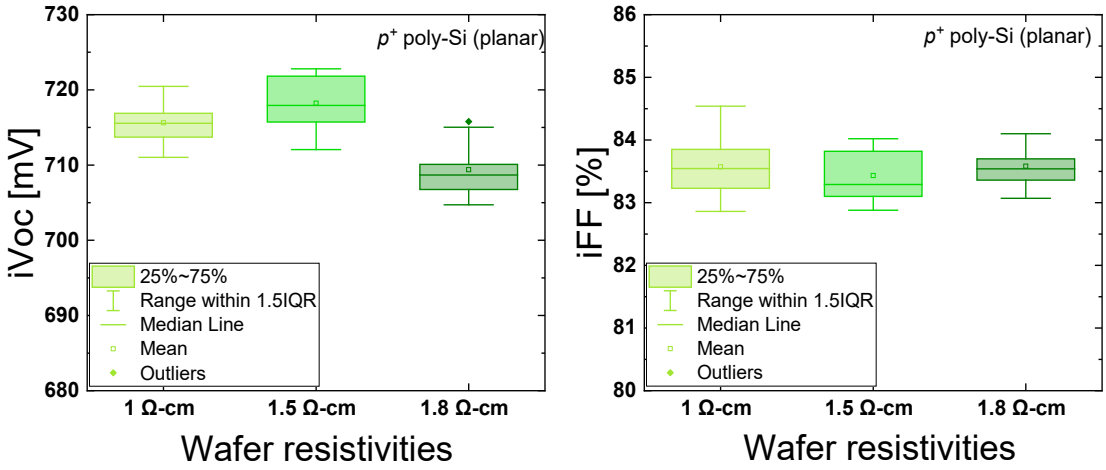

Figure 5. *QSSPC derived properties of 250 nm p⁺ poly-Si layers on symmetrical planar test samples. a) iV_{oc}, b) iFF.*

Figure 6 shows the iV_{oc} and iFF values of the c-Si surface obtained after etching the n⁺ poly-Si deposited on the textured surface. As expected, without the passivating effect offered by the poly-Si layers, the surface passivation degrades, and ranges from 690-705 mV.

However, some improvements in passivation were observed as compared to the textured c-Si wafer which did not undergo the poly-Si process, where the iV_{oc} was limited to 670-680 mV. This could be attributed to the diffusion of dopants into the c-Si from the n^+ poly-Si layer during the high temperature annealing process, which leaves behind a shallow dopant profile after the poly-Si has been etched. This could improve the surface passivation by providing the front surface field while not contributing to excessive Auger recombination [16].

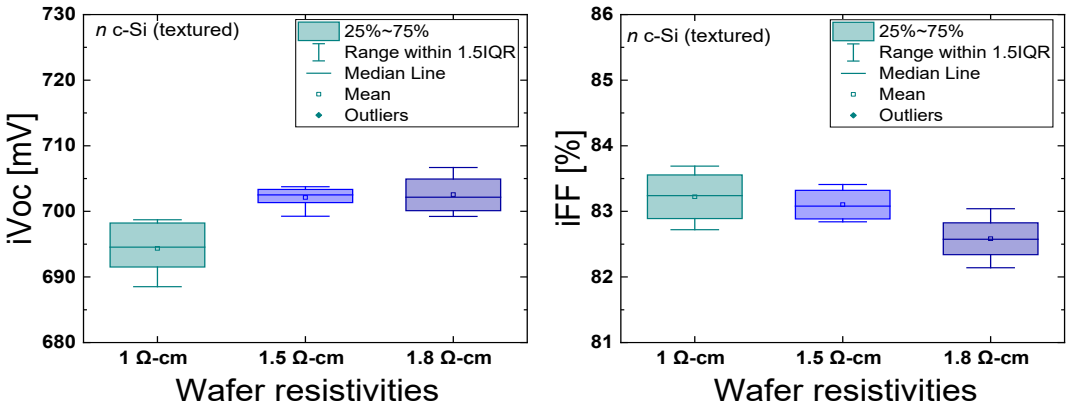

Figure 6. *QSSPC-derived properties of textured surface of c-Si samples obtained after etching the n^+ poly-Si layer. a) iV_{oc}, b) iFF.*

Figure 7 shows the bulk saturation current density ($J_{0,bulk}$) of the wafers with different resistivities for three different conditions – with n^+ poly-Si, with p^+ poly-Si and n-c-Si (textured) after removing the etched regions. It was observed that the absolute values of the bulk J_0 recorded in each of these cases were different, however the trend in the $J_{0,bulk}$ remains similar. It was observed overall that the wafers with the highest resistivities recorded generally higher $J_{0,bulk}$ across different conditions. The $J_{0,bulk}$ was lowest for samples with n^+ poly-Si (in the 15-30 fA/cm^2 range), where higher $J_{0.bulk}$ was observed for wafers with higher resistivities (1.8 Ω-cm). The values of $J_{0,bulk}$ for samples with p^+ poly-Si were observed to be in the range of 20-50 fA/cm^2, with wafers with higher bulk resistivities featuring higher $J_{0,bulk}$. However, for the samples where n^+ poly-Si was etched, the $J_{0,bulk}$ was found to be as high as 80 fA/cm^2 for the wafers with higher resistivities (1.8 Ω-cm). The $J_{0,bulk}$ is usually related to the wafer quality and the trap densities in the mid-level injection range. The $J_{0,bulk}$ may also be impacted by the high temperature diffusion process. The precise explanation of the difference in the $J_{0,bulk}$ values for different conditions requires further investigation and is beyond the scope of this work.

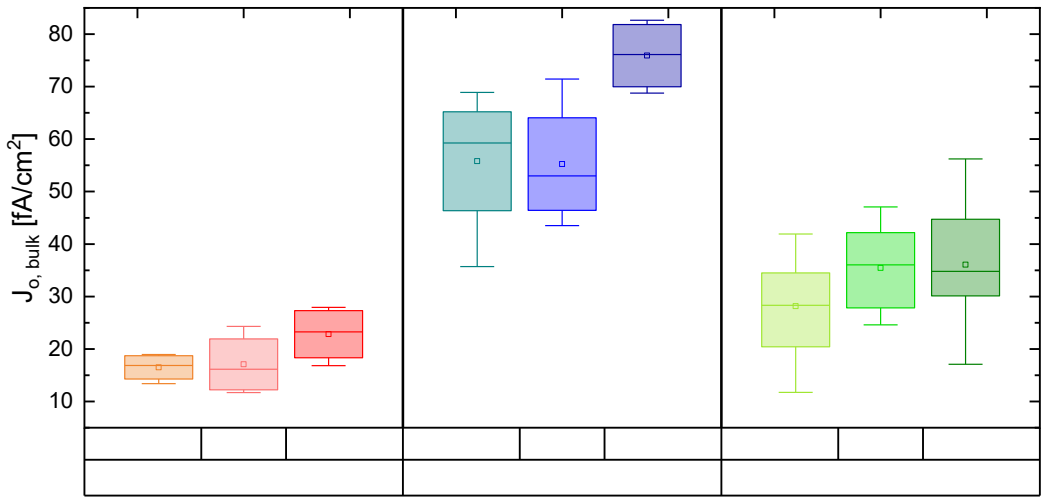

Figure 7. *QSSPC-derived $J_{0,bulk}$ of c-Si samples obtained for symmetric n^+ poly-Si, p^+ poly-Si and n-c-Si (textured) after etching the n^+ poly-Si for wafers with different resistivities.*

3.3 Solar cell characterization and loss analysis

Solar cells with double-side passivated contacts were fabricated according to the process explained in detail in [4]. The passivation properties of the solar cell precursors (without metallization) were also ascertained by QSSPC of several non-metallized solar cell precursors after a high-temperature firing process mimicking the metallization process. Figure 8 shows the iV_{oc} and iFF of the solar cell precursors as obtained by QSSPC measurements, after the simulated firing at high temperature.

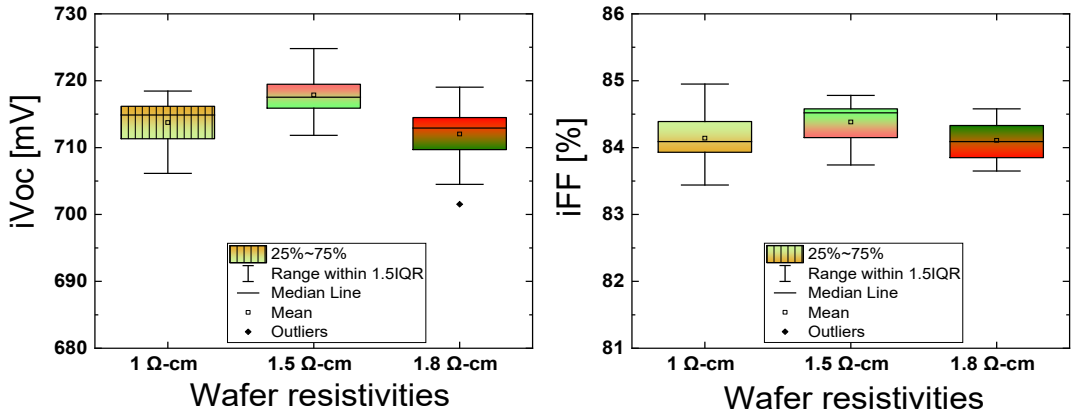

Figure 8. *QSSPC-derived properties of unmetallized solar cells precursors (without metallization) after a simulated high-temperature firing process. a) iV_{oc}, b) iFF.*

The measured 1-Sun J-V parameters (V_{oc}, J_{sc}, FF, efficiency) of the solar cells are plotted in Figure 9. The champion solar cell achieved an efficiency of 21.9%, with a V_{oc} of 685 mV, J_{sc} of 39.5 mA/cm^2 and FF of 81%. All solar cells had a V_{oc} in the 680 - 688 mV range. The solar cells fabricated with wafers with highest resistivity (1.8 Ω-cm) exhibited slightly lower V_{oc} values (mean V_{oc} 682 mV), while those fabricated with wafers having resistivities closer to 1.5 exhibited the highest V_{oc} of 688 mV, while the average V_{oc} for solar cells fabricated on the wafers with resistivities 1 and 1.5 Ω-cm was similar (≈ 685 mV). The loss in V_{oc} is mostly attributed to the inferior passivation of the etched regions between the n^+ poly-Si fingers. The n^+ poly-Si fingers covered approximately 12% of the front surface, while the area where the poly-Si was etched covered the remaining 88%. The area normalized $J_{0,metal}$ for the Ag contacts to the front were ≈ 220 fA/cm^2 while that of the Ag-Al contacts to the p^+ poly-Si on the rear were ≈ 200 fA/cm^2. The metal fraction on the front is ≈ 2% while on the rear is 4%. The combined loss in V_{oc} from metallization is ≈ 10 mV, however, the solar cells lose 15 - 20 mV after metallization. The difference is attributed to the uneven surface on the front which may lead to a greater deterioration in the passivation of the non-metallized regions.

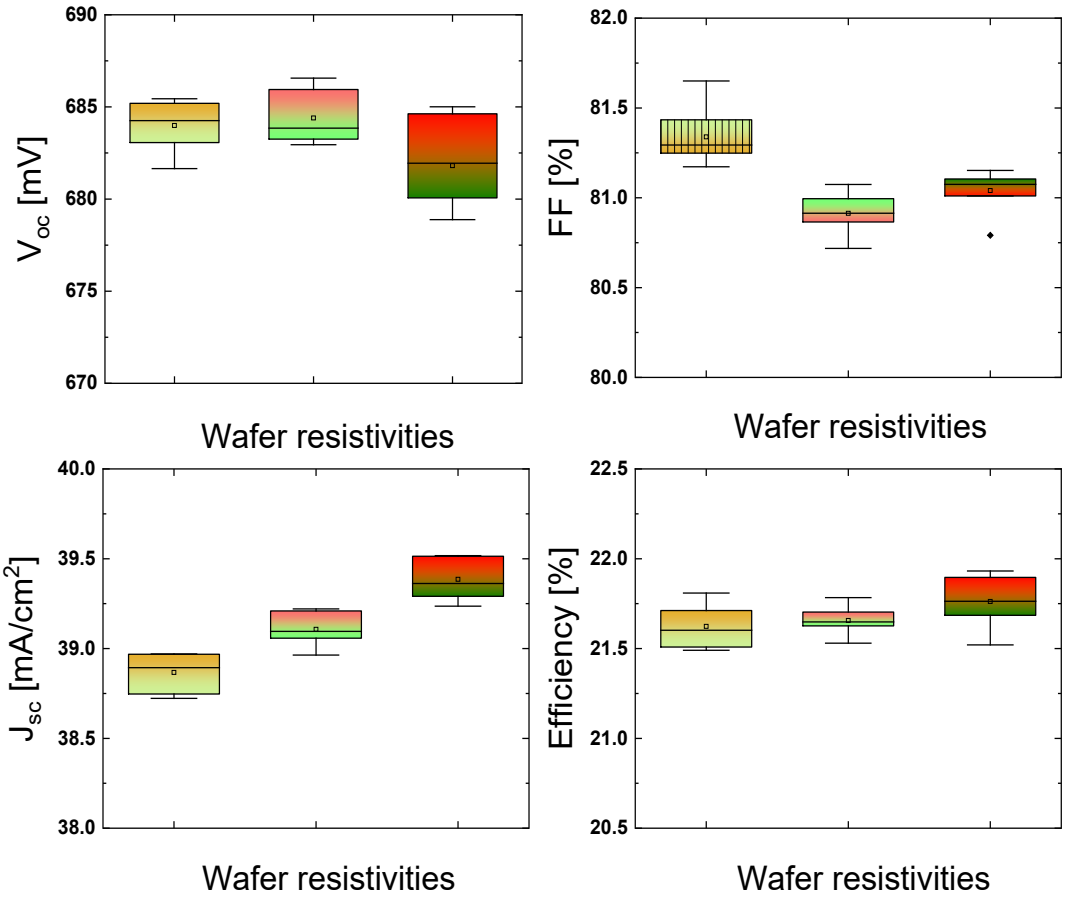

Figure 9. *Measured J-V parameters of double-side passivated contact solar cells fabricated on wafers with different resistivities. a) V_{oc}, b) FF, c) J_{sc}, d) Efficiency.*

Figure 10 shows the series and shunt resistances (R_s, R_{sh}) of the solar cells obtained from the J-V analysis. From the R_{sh} plot it is clear that none of the solar cells was shunted. This provides confidence in the fabrication process. High R_{sh} is crucial to the reverse bias performance of the solar cells which is an important factor for any commercial PV technology [17]. The R_s was lowest for the solar cells fabricated on the 1 Ω-cm wafers, which resulted in the high FF in these solar cells.

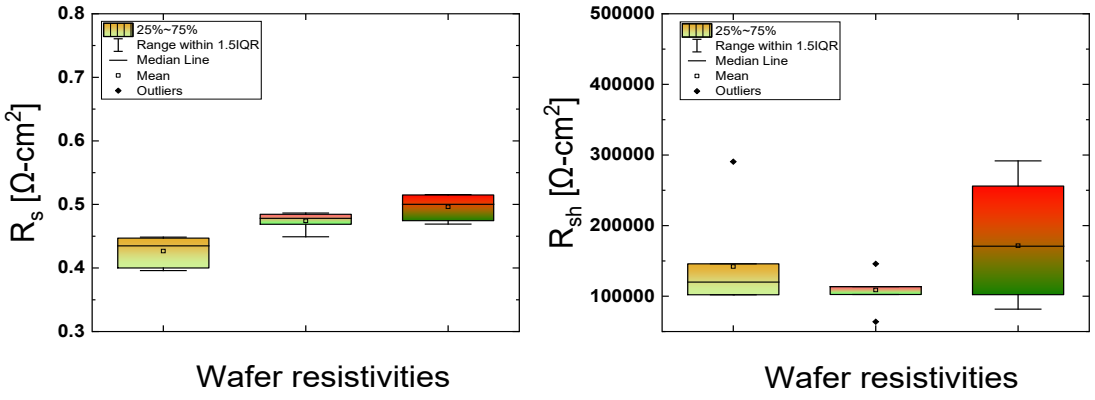

Figure 10. *Series (R_s) and shunt (R_{sh}) resistances of the solar cells obtained from the J-V measurements.*

A FF loss analysis was done according to the method described in [18]. The different components of the FF loss are shown in Fig. 11. It can be seen that the R_s is the major factor limiting the cells' FF. The FF loss due to R_{sh} is negligible, which is evident from the high values of R_{sh}. However, the FF loss due to the non-ideal recombination was smallest in the wafers with resistivity ≈ 1.8 Ω-cm, while it was highest in the wafers with resistivity 1.5 Ω-cm. To analyse the factor contributing to the non-ideal recombination (J_{02}), similar cells fabricated with a different Ag-Al metal paste for contacting p^+ poly-Si on the rear side were analysed (Figure 12). Paste P1 is used for all the solar cells presented in this work. The second paste (P2) had lower Al content than the first (P1). It was observed that although the contacts properties of the other paste were poor, it resulted in reduction in FF loss due to J_{02}. Although the same set of metallization pastes was used for all solar cells, the values of the FF loss due to J_{02} were different for the solar cells fabricated. Hence, it can be inferred that metallization process, among other factors such as deep state traps and non-uniformity in wafer quality, contributes to the non-ideal recombination losses [19], [20].

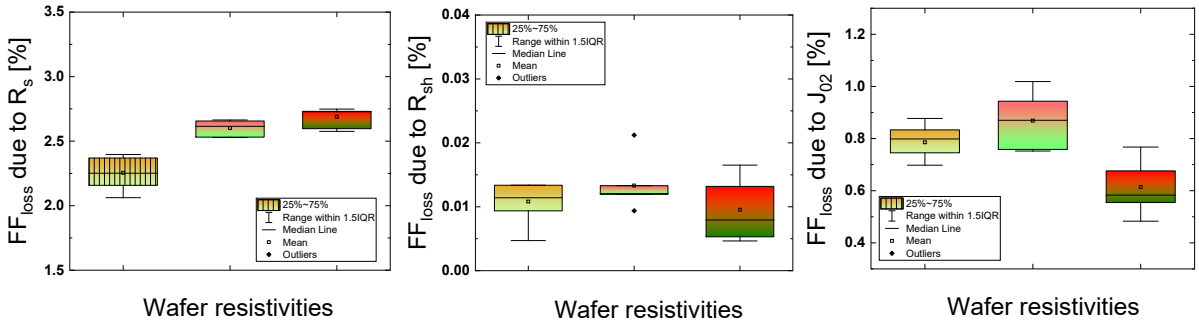

Figure 11. *Components of the FF loss obtained from the FF loss analysis of the solar cells. a) FF loss due to R_s, b) FF loss due to R_{sh}, c) FF loss due to J_{02}.*

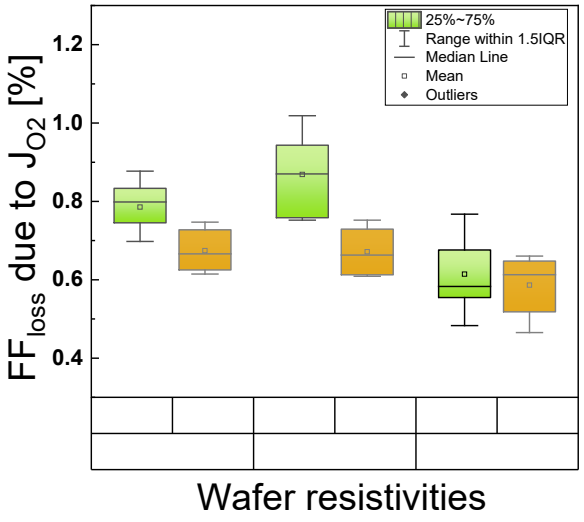

Figure 12. *FF loss due to J_{02} obtained from the FF loss analysis of the solar cells for two different Ag-Al pastes used (P1 and P2) to contact the p^+ poly-Si on the rear side of the solar cells. Paste P1 was used for all solar cells reported in this work.*

To further understand the impact of metallization on the R_s and consequently FF, the ρ_c for the front and rear contacts were evaluated. Figure 13 shows the ρ_c for the front Ag contacts to n^+ poly-Si fingers on textured surface at the front side and Ag-Al contacts to p^+ poly-Si on the planar surface at the rear. It can be seen that the ρ_c for both front and rear contacts are similar for all fabricated solar cells. However, in Figures 10 and 11, the R_s and FF loss due to R_s were observed to increase with increasing wafer resistivities. Hence, it can be concluded that the differences in the R_s values of the cells arise from the difference in the wafer resistivity.

We believe the wafer resistivity plays a role here due to the solar cell architecture on the front side involving heavily doped poly-Si fingers, but extremely lightly doped field regions. Additionally, for solar cells with emitter on the rear, wafer resistivity is thought to play an important role in charge carrier transport [21]. The average ρ_c for the Ag contacts to n^+ poly-Si were marginally better than that for Ag-Al contacts to p^+ poly-Si. While similar observations were reported earlier [22], the ρ_c values for Ag contacts to n^+ poly-Si have been reported to be $\simeq$ 0.5 to 2 mΩ-cm^2. The contact resistivity is highly sensitive to the paste chemistry and this could be a reason for the increased ρ_c [23]. Nevertheless, improvement in the metallization process has been shown to improve the R_s, which improves the FF and the cell efficiency [24].

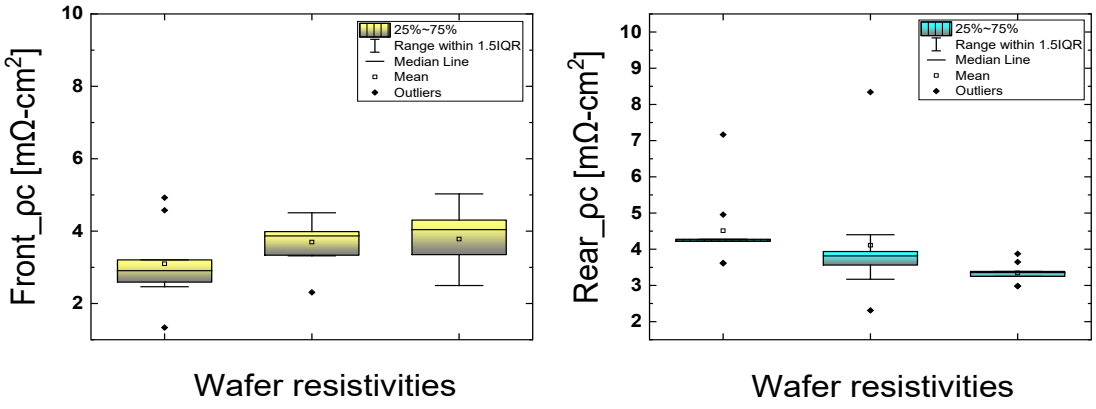

Figure 13. *Specific contact resistivity for (a) the front and (b) the rear FT contacts to the n^+ poly-Si (front, textured) and p^+ poly-Si (rear, planar) obtained from the fabricated solar cells.*

To understand the loss in the J_{sc}, the External Quantum Efficiency (EQE) of the solar cells was plotted as a function of the wavelength, see Figure 14. Spots between the poly-Si fingers on the front were chosen for the EQE measurements. From Figure 14, the J_{sc} trend observed in Figure 9 can be explained. The wafers with the lowest resistivities exhibited a slightly lower EQE in the 400-900 nm range, which causes the lower J_{sc} of the final solar cells. The reflectance of the solar cells on highest resistivity wafers was also marginally lower than that for the wafers with lower resistivity. This also led to minor improvements in the loss from the front side which could enhance the current. The EQE marginally improved for the solar cells fabricated on wafers with higher resistivities, and the observation correlated with the measured J_{sc} data of the solar cells. Furthermore, the J_{sc} loss analysis was done as reported in [4]. The different components of the J_{sc} loss are shown in Figure 15. It can be observed that different components of the J_{sc} loss are similar for the solar cells fabricated on wafers with different resistivities except for the base collection loss. The trend in the base collection loss component agrees with the trend observed in the J_{sc} of the solar cells. Additionally, the wafers with the lowest resistivity suffered from additional blue loss and parasitic absorption which resulted in further lowering of the J_{sc} in the respective solar cells. While the precise reason for the marginally improved EQE and reflectance performance of high resistivity wafers is not known, we hypothesize that the surface of the high resistivity wafers was different (slightly rougher) compared to the wafers with lower surface resistivity. This would also explain the slightly lower iV_{oc} of the high-resistivity samples, and the slightly lower contact resistivity of the Ag-Al contacts to p^+ poly-Si on the rear surface, as rougher surfaces usually lead to lower V_{oc} and improved contact properties [9].

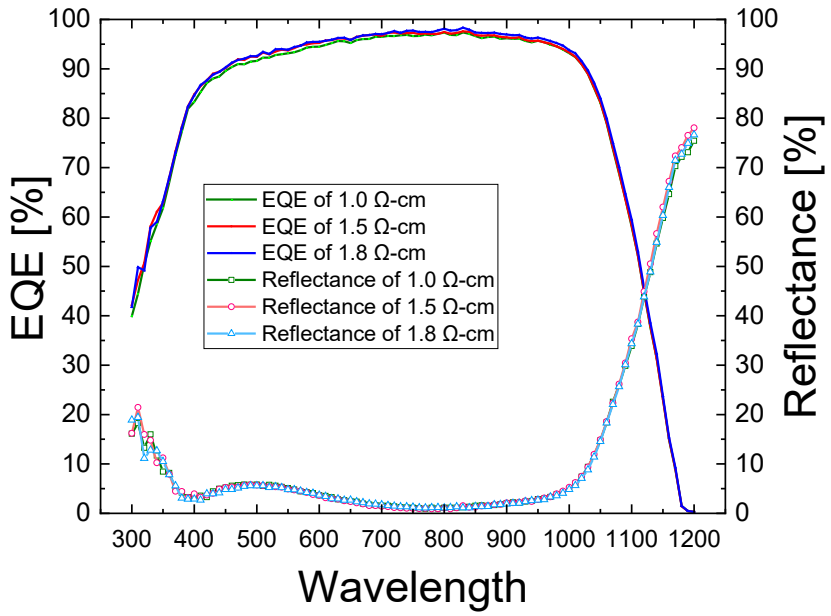

Figure 14. *Spot EQE and reflectance of the solar cells with double-side passivated contacts for different wafer resistivities. The spot for the EQE was chosen in the wing region between the poly-Si fingers on the front.*

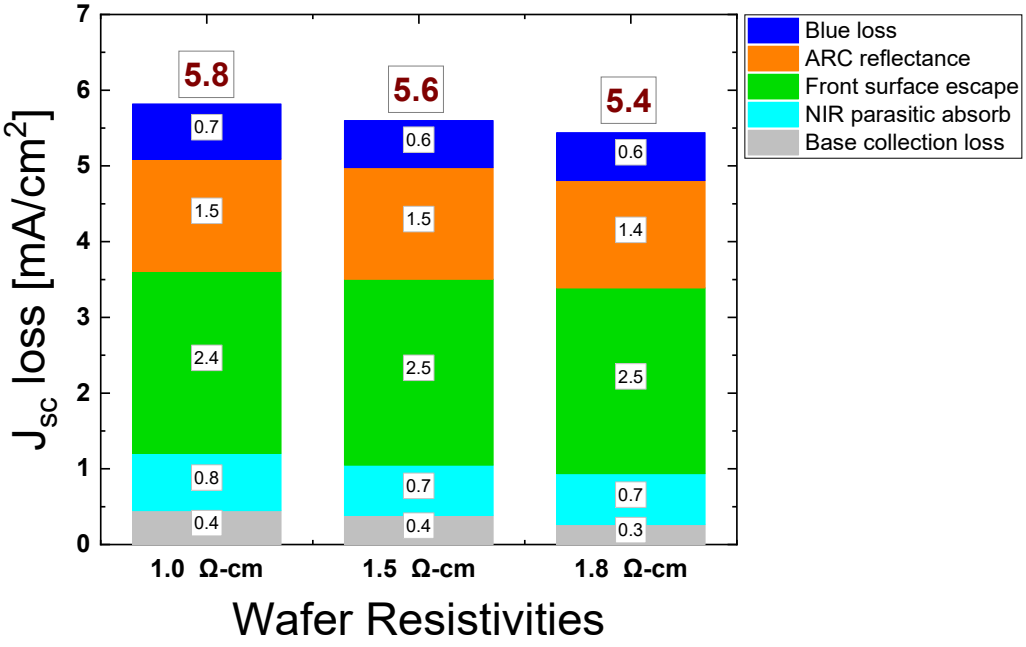

Figure 15. *Components of the J_{sc} loss for the double-side passivated contact solar cells fabricated on wafers of different resistivities.*

4. Conclusion

In this work, large-area silicon solar cells featuring poly-Si based passivated contacts on both the front and rear side of the solar cells were fabricated and characterized. The cells were fabricated in the rear-junction configuration on n-type wafers having different wafer resistivities, to examine the impact of wafer resistivity on the solar cell performance. The n^+ poly-Si on the front side was patterned using an ink-jet process to limit the poly-Si to the regions under the metal contacts. This was done to reduce the $J_{0,metal}$ from the front contacts. The rear side

featured p^+ poly-Si on the entire surface. The solar cells fabricated on the wafers with highest resistivities achieved 22% efficiency on large area using high-temperature FT metallization. The device performance was found to have a strong dependence on the wafer resistivities. While both V_{oc} and FF reduced for solar cells fabricated on wafers with high resistivities, the improvement in the J_{sc} more than compensated for that. The V_{oc} was found to decrease with increased wafer resistivities, which could be attributed to the difference in wafer surface arising from a difference in response to chemical processing and possible differences in the wafer qualities. The FF also decreased for solar cells on high resistivity wafers. With detailed characterization, it was found that increased wafer resistivity contributed strongly to the overall series resistance of the solar cells, leading to lower FF values. On analysis of FF, wafer resistivity was observed to impact on the series resistance, where the R_s increased with increasing wafer resistivity. Hence, while the wafer resistivity could have an impact on the R_s and the wafer quality, the metallization could impact the J_{02}. The J_{sc} exhibited a trend of slightly increasing with increasing wafer resistivity. The increase in J_{sc} was attributed to the higher generation current and the lower losses in the bulk, and reflection from the front surface. This is also attributed to the perceived differences in the wafer surface. Detailed loss analysis was performed to investigate the sources of losses limiting the device efficiencies. It was found that the front side wing regions (without the poly-Si) were the major source of recombination limiting the device efficiency. It was also found that the metallization contributed strongly to the non-ideal recombination in the solar cells, which along with wafer resistivity, impacted both the V_{oc} and the FF. However, further research to understand the sources of these limitations and ways to overcome them could enable cell efficiencies beyond 25% [25].

Data availability statement

Most of the data used for the current work has been included in the manuscript. Any additional data can be made available upon request to the authors.

Author contributions

P. Padhamnath was responsible for the conceptualization, investigation, formal analysis and validation of the experiments and the writing of the original draft. G. De Luna was responsible for the investigation, visualization, validation and formal analysis of the experiments and helped with the writing of the original draft. R. Zhong and J.D. Arcebal helped with the investigation, visualization and validation of the data and results. A. Rohatgi and A.G. Aberle were responsible for funding acquisition, project administration, provision of resources and for reviewing and editing the manuscript.

Competing interests

The authors declare that they have no competing interests.

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Legal Disclaimer

The views expressed herein do not necessarily represent the views of the U.S. Department of Energy, the United States Government, National Research Foundation Singapore (NRF), the Energy Market Authority of Singapore (EMA) and Singapore Economic Development Board (EDB).

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