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Understanding and Minimizing Perimeter Losses of Silicon-Based Monolithic Tandem Solar Cells – A Simulation Study

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Abstract. The vast majority of monolithic perovskite-silicon-based tandem cells to date is manufactured in R&D environments using small scale perovskite top cells (~1-4 cm²), typically placed on a larger silicon bottom cell. The high perimeter-to-area ratio leads to significant perimeter losses, which limit the maximum achievable efficiency and complicates loss analysis for further design optimization. An understanding of perimeter loss mechanisms and design rules for their minimization is therefore important for effectively progressing high efficient tandem solar cells in R&D. In this work we perform a 3D device simulation study of perimeter losses in an exemplary perovskite-silicon tandem solar cell. The impact of structuring the various laterally conducting layers, i.e. at the front and rear side as well as between the sub cells, on the perimeter efficiency loss is systematically investigated. We thereby identify the fundamental mechanisms of carrier transport into the perimeter, and clarify the impact of the silicon and perovskite absorber, the various laterally conducting layers, as well the electrical connection of the sub cells. We find that in each sub cell at least one carrier type must be hindered to be conducted into the perimeter. This is however complicated by the fact that this parasitic lateral transport can also be provided by “bordering” conductive layers connected via the tunnelling or recombination junction. Promising structuring variants and general design rules to achieve low perimeter losses with low structuring effort are then derived from the results. The losses are quantified to range from ~0.2 – 4%$_{abs}$ for a 1 cm^2 top cell size, with the lowest values representing an unavoidable loss from the Si wafer conductance which is present also in champion cells with high structuring effort.

Keywords: Tandem Solar Cell, Perimeter Loss, Simulation

1. Perimeter loss mechanism and simulation setup

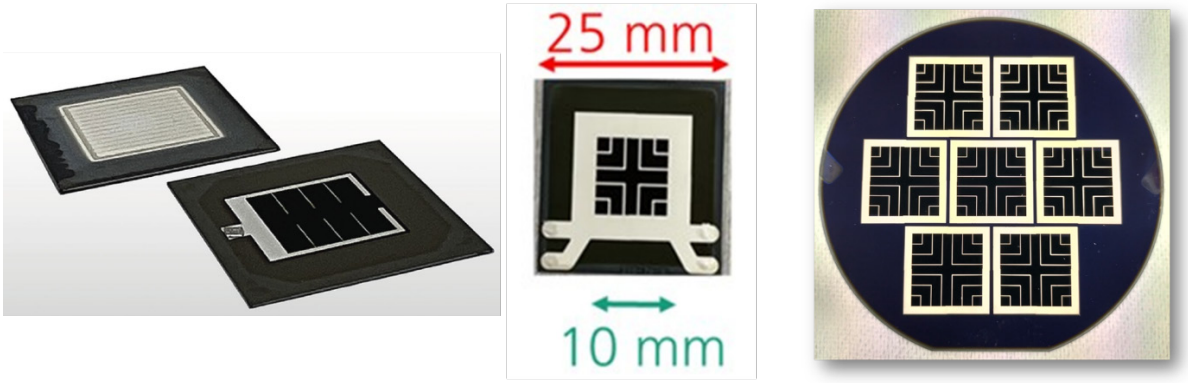

***Figure 1. Left**: 1 cm² top cell on 2.1 cm x 2.1 cm bottom cell design by KAUST [1]; **middle**: 1cm x 1cm top cell on 2.5cm x 2.5 cm Si bottom cell with laser cut unpassivated edge by Fraunhofer ISE [2]; **right**: seven 2cm x 2cm top cells on one 4" Si bottom cell by Fraunhofer ISE*

Most commonly, laboratory perovskite-silicon tandem cells are designed by using a full-size silicon bottom cell and defining a smaller active tandem cell area via the front metallization and optionally by structuring other layers. The cells are either left in the host wafer, or cut into individual cells at some distance from the active cell area, see **Figure 1**. The latter introduces additional recombination at the physical edges. During IV measurement only the active cell area is illuminated, and the perimeter represents a dark cell area connected in parallel to the active cell area causing recombination losses. It is shown experimentally that without structuring some conductive layers in the perimeter, the tandem efficiency can be reduced by ~3% abs [3].

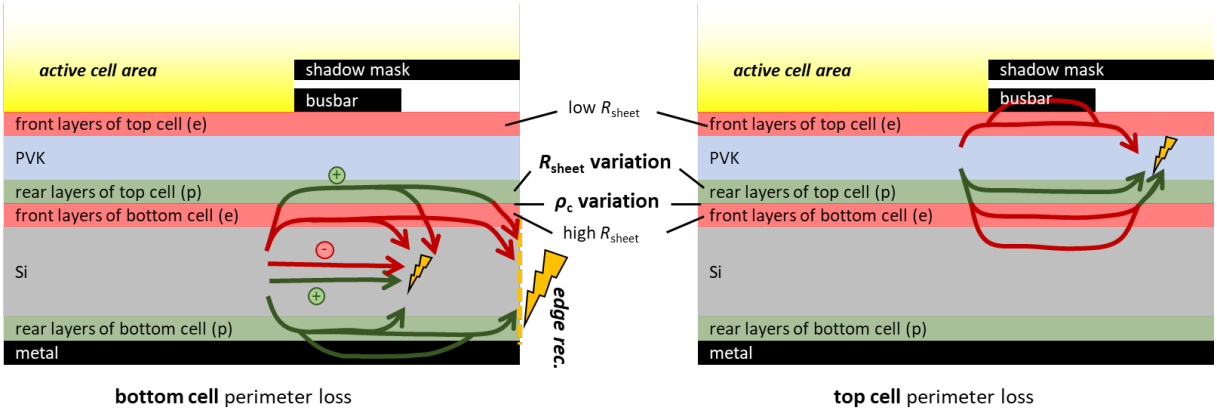

***Figure 2.** Carrier transport paths to the recombination sites in the dark perimeter for holes (green) and electrons (red); **left**: bottom cell perimeter losses; **right**: top cell perimeter losses*

In **Figure 2** all possible carrier transport paths from the active cell area into the recombination sides in the dark perimeter are sketched for an unstructured design. For the case that the sub-cell is not cut from the host wafer or an efficient edge passivation is applied, the edge recombination component would not be relevant. The figure and the following discussions are exemplary for the case of bottom cell with rear HTL and front ETL and a top cell with a rear HTL and ETL at the front, i.e., a "pin" top cell, but are equivalently valid also for the inverse structure. For understanding the fundamental perimeter loss mechanisms, the tandem cell is conceptualized into the respective main absorber, and the layers contributing to lateral electron and hole conductance. In practice, the conductance of the "front layers of top cell" is fully dominated by the front TCO, for which a low R_{sheet} of 80 Ω/□ is assumed. Lateral conductance of the perovskite absorber is assumed to be negligible, due to being very thin and also having

lower carrier mobilities compared to silicon. The low conductivity effectively also suppresses recombination losses at the physical edge of the perovskite absorber, which is consequently not considered in **Figure 2** and the following simulations.

The intermediate layers “rear layers of top cell” and “front layers of bottom cell” are separated by the “junction resistance” ρ_c, which is assumed to have a low value in the active cell area, but is varied in the perimeter to represent isolation between the top and bottom cell as indicated in **Figure 2**. In our simulations the “front layers of bottom cell” are assumed to have a very high R_{sheet} of 10^4 Ω/□, which is well representative of the nanometre-thin silicon thin films in typical silicon heterojunction (SHJ) bottom cells. The R_{sheet} of the “rear layers of top cell” are varied in our simulations. In practice, these layers comprise the lowly conductive HTL, and any other intermediate layers above the “junction resistance” ρ_c. Notably, the location of the junction resistance does not necessarily coincide with the location of the recombination or tunnelling process taking place, which is important to consider when judging the impact of lateral conductance of a particular material layer. For instance, when using a recombination TCO, the dominating resistance could be located at the a-Si / TCO interface instead of the TCO / HTL interface, in which case the recombination TCO’s lateral conductance must be attributed to the “rear layers of top cell” and be thus detrimental for perimeter losses. Also it is noted that in a currently less common inverted tandem configuration with a “nip” top cell, the attribution of the lateral conductance of the intermediate layers to the top or bottom cell could be altered.

To understand the various parasitic current paths into the perimeter, it is helpful to distinguish recombination losses happening in the bottom cell and top cell, respectively. For the **silicon bottom cell**, both electrons and holes can diffuse laterally within the wafer to recombine within the perimeter (**Figure 2** left). Additionally, electrons and holes can be transported via the front and rear conducting layers, respectively. Notably, these layers are connected in parallel to the silicon wafer lateral conductance. Even when using a front p/n-junction bottom cell design, the minority carrier photo-conductance in the silicon wafer is still connected in parallel to these layers, which is typically in the order of 10^3 Ω/□ at maximum power conditions. This value thus represents an upper limit of achievable effective R_{sheet} for electron transport in the bottom cell, meaning that engineering R_{sheet} values for the front side of bottom cells much higher than this value does have only minor impact on suppressing perimeter losses. A less intuitive path for bottom cell perimeter losses exists for electrons: as indicated on **Figure 2 left**, they can be effectively transported via holes in the “rear layers of top cell”, as they are electrically connected via the tunnelling or recombination junction. Notably, bottom cell recombination losses happen both in the area of the perimeter, and also at the edge if the cells are cut. For the **top cell**, which is much thinner, conductance within the absorber is negligible, and so lateral transport only happens within the adjoining conductive layers. As indicated in **Figure 2** right, holes can also be transported via electrons in the bottom cell by being connected via the junction. Notably this can happen not only via the front layers of the bottom cell, but also via the electron conductance of the silicon wafer, which may be minorities or majorities depending on the doping type. For typical thin top cell materials like a perovskite absorber, edge recombination can usually well be neglected.

Other parasitic perimeter and edge effects might be caused by shunt paths from edge deposition of the electrodes (TCO, metal) or structuring-induced shunts and recombination (e.g. scratches from shadow mask). Such effects are not considered explicitly in this study, but are likely suppressed as well by the suggested measures.

As recombination in the dark perimeter requires both electrons and holes, it is obvious that the suppression of lateral conductance of **one** carrier type in each sub cell is required and sufficient to effectively minimize perimeter losses. However, this is not trivial in particular because of the current paths crossing the junction, and because of the inability to prevent lateral carrier transport in the silicon wafer. The unavoidable presence of recombination sites in the dark perimeter facilitates this “conductance enhanced recombination” [4] especially at the physical wafer edge for a cut bottom-cell.

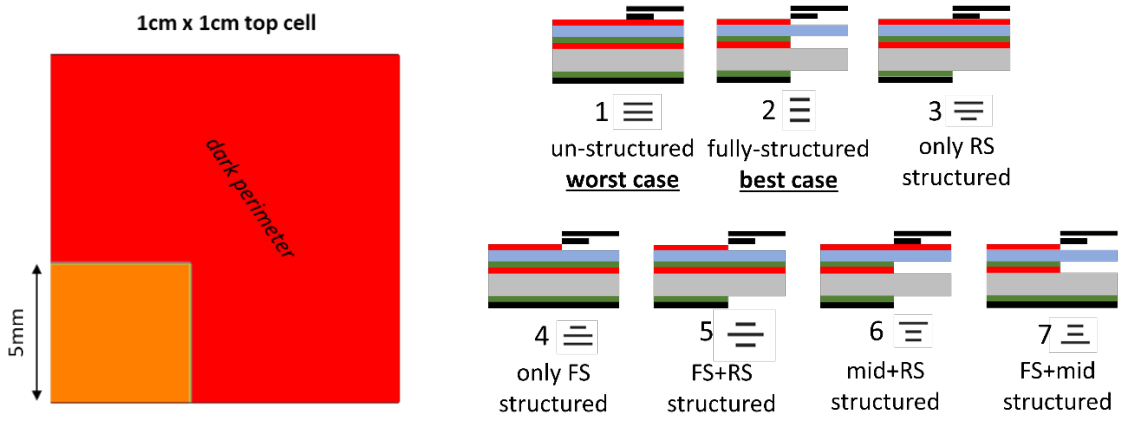

***Figure 3. left**: 3D quarter-cell symmetry solution domain as used in Quokka3; **right**: 7 structuring variants investigated in the simulation study; structuring means setting a very high R_{sheet} in the perimeter, i.e., disabling the lateral conductance of the respective layer (meaning of layer colors see **Figure 2**)*

In this work we use the tandem functionality of the solar cell simulation software Quokka3 [5] to perform 3D simulations of tandem cells with an active area of 1cm x 1cm within a bottom cell size of 2.5cm x 2.5cm, see **Figure 3 left**. The basic electro-optical cell properties are taken from [5]. Keeping the properties in the active cell area constant, we vary the perimeter properties to represent a systematic variation of structuring the laterally conducting layers.

In **Figure 3 right** an overview of the investigated structuring variants is given. As long as the front layers of the bottom cell and the rear layers of the top cell are electrically well connected in the perimeter, i.e. have a low junction resistivity, there are essentially 3 layers which can be structured in the perimeter to disable their lateral conductance: the front layers, the rear layers (including metallization) of the bottom cell, and the entity of all intermediate layers, here represented as the “rear layers of top cell”, see also explanation above. Additionally we vary the sheet resistance of the “rear layers of top cell”, in order to investigate the possibility of minimizing perimeter losses by using lowly conductive intermediate layers instead of structuring. Furthermore we vary the bulk doping type between n-type and p-type, effectively switching between a front p/n-junction (FJ) and p/n-rear junction (RJ) bottom cell. We also vary the junction resistivity in the perimeter, i.e. the electrical connection quality of the sub cells, which may be a deliberate or side-effect from the structuring intermediate layers like the recombination TCO. Finally, we simulate all cases with and without edge recombination, the latter being more representative for non-cut-out cells still residing in the host bottom cell. As explained above, edge recombination is only applied to the silicon bottom cell, using worst-case edge recombination properties as published in [6] to represent a clean cut and fully unpassivated edge.

Notably, the simulations assume unchanged layer and interface properties in the perimeter, except for the lateral conductance of the structured layers, meaning that any potential influence of structuring on recombination properties is not considered. This could be electric passivation layers with different recombination compared to the active area or structuring-induced scratches (e.g. shadow mask)-.

2. Results and discussion

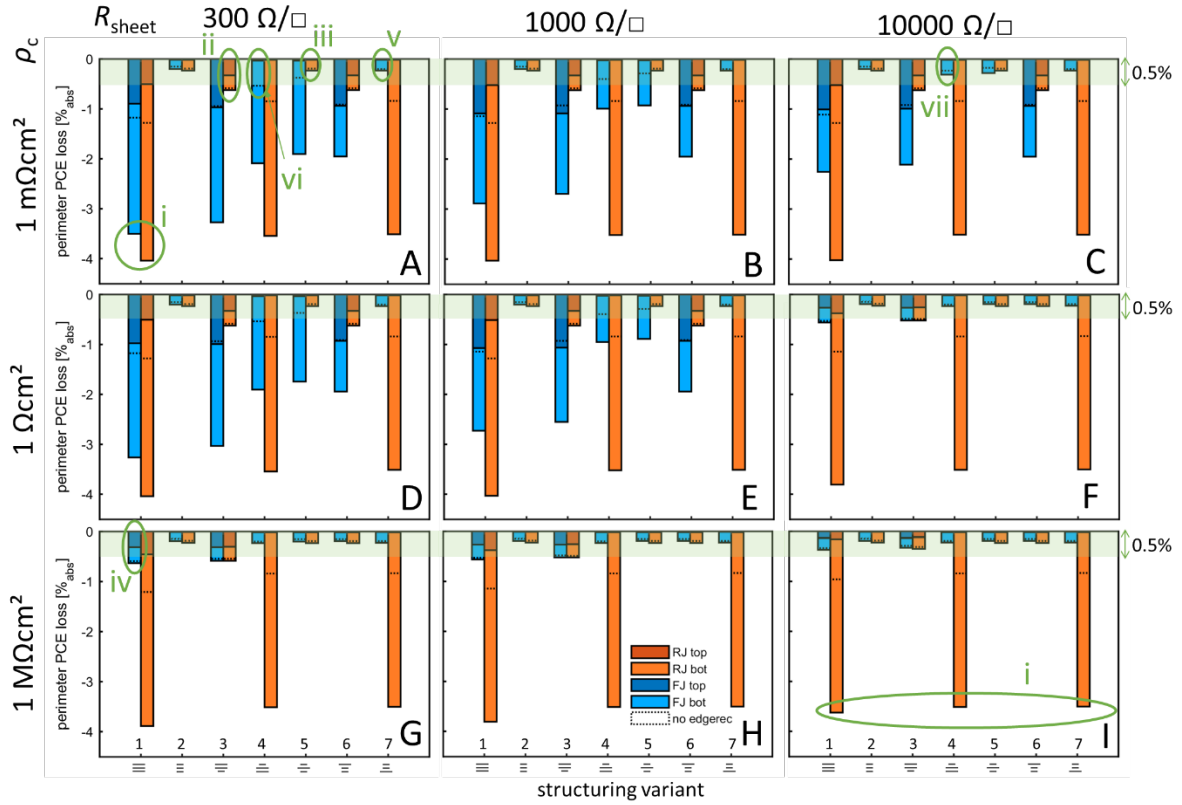

Figure 4. *Perimeter efficiency loss for the 7 different structuring variants; different shades distinguish losses originating from the top (top) and bottom (bot) cell, respectively; dashed lines indicate the loss without edge recombination; red means rear junction (RJ) and blue means front junction (FJ) bottom cell; with variation A-I of perimeter junction resistivity ρ_c and perimeter "rear layers of top cell" R_{sheet}.*

In **Figure 4** an overview of the losses for the various structuring variants is shown. The perimeter power conversion efficiency (PCE) loss is calculated by comparing the respective simulated efficiency with a perimeter-loss-free reference efficiency, which is simulated by restricting the simulation to the active cell area only, and assuming ideal non-recombining edges.

Firstly, we emphasize a well-known requirement from single junction silicon devices which also applies to Si based tandems, namely that a conductive emitter (and metallized) region in the dark perimeter must strictly be avoided [7]. More precisely, the effective R_{sheet} of all emitter-side layers must be significantly larger than the effective R_{sheet} of minority carriers in the bulk at maximum power conditions. The latter can be estimated to be in the order of 10^3 Ω/□, meaning that the perimeter emitter R_{sheet} should be few times this value. Notably, aiming for even higher R_{sheet} would not bring additional benefits for suppressing edge losses, as then lateral conductance is fully taking place in the Si bulk anyway. For SHJ bottom cells, when omitting the TCO layer, this requirement is well fulfilled due the thin silicon layers forming the p/n junction. When instead a poly-Si bottom cell technology is used, care should be taken to fulfill the mentioned R_{sheet} requirement.

For further discussion we focus only on distinct variations. It can be seen that for this specific cell size of 1 cm^2 on 2.5 cm x 2.5 cm bottom cell, the perimeter loss can be up to ~4 $\%_{abs}$ on cut-out cells if no measures are taken, which is inline with published experimental results [3]. This loss is dominated by edge recombination in the bottom cell, and is only that high when using a rear junction cell without any structuring of the conductive rear side layers (eg. i in **Figure 4**). For a front junction cell this loss is already reduced, which however requires

a low lateral conductivity of the front side of the bottom cell then forming the emitter as assumed in our simulation setup. Without edge recombination, which also is representative of the case of non-cut-out tandem cells still residing in the host bottom cell, the perimeter losses can still be high with >1 $\%_{abs}$. Even for the best case scenario, there is a fundamentally unavoidable bottom cell loss of ~0.2 $\%_{abs}$, which is caused by the lateral conductance of the silicon wafer. This loss is also present in record devices with high structuring effort. The exact value depends mainly on the wafer resistivity and thickness.

To suppress perimeter losses to below ~0.5 $\%_{abs}$, some structuring of the conductive layers is required. Notably, in the case of such a suitable structuring, edge recombination is effectively shielded in most cases, meaning that for a structured design there is generally little difference in perimeter loss whether the cell is cut-out or not. We identify 3 different ways to suppress parameter losses below 0.5 $\%_{abs}$ potentially **requiring structuring of a single layer only**:

- **Figure 4 (ii)**: **Rear side structuring only,** i.e., rear emitter and rear metal structuring when using a rear junction bottom cell; inversely, using a rear junction bottom cell without rear structuring inevitably leads to high perimeter losses **(i)**. Practically, the use of a shadow mask for TCO + metal windows only in the active area is applied in SHJ cells [1] and a laser process to create a passivated mesa trench forming a floating rear emitter in the perimeter for homojunctions [3]. This is typically combined with structuring the front side TCO using a shadow mask to overcome the remaining top cell losses **(iii)**.
- **Figure 4 (iv)**: Using a front junction bottom cell **structuring only the recombination** / tunnel **junction** to achieve high "junction resistance" ρ_c in the perimeter, i.e. electrical isolation between top and bottom cell in the perimeter; notably, ρ_c in the perimeter must be very high (> 10^4 Ωcm^2), which is in contrast to shunt-quenching requiring only moderate increase of ρ_c to decouple the transport through the bottom cell [8]. The use of a shadow mask for recombination TCO deposition only in the active area and a poor contact between TCO-less SHJ front emitter and the HTL in the perimeter might be a practical approach here. This can be combined with structuring the front side TCO minimizing top cell losses [2] **(v)**.
- **Figure 4 (vi)**: Using a front junction bottom cell, **structuring only the front side TCO,** if the cell remains within the host wafer or efficient edge passivation is ensured. If edge recombination is involved it only works in combination with reasonably high R_{sheet} of all intermediate layers (> 10^3 $\Omega/\square$) **(vii)**.

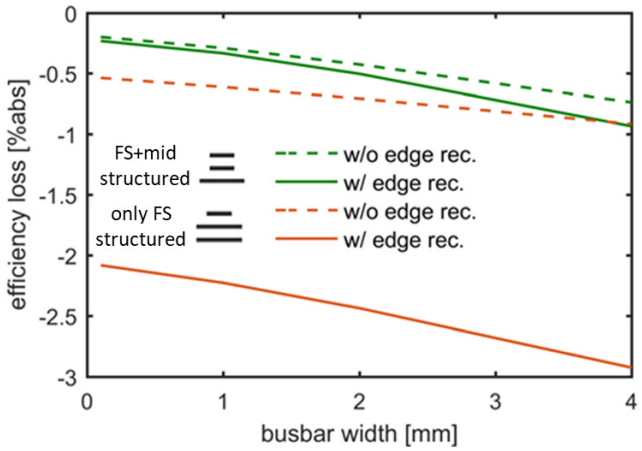

Figure 5. *Perimeter efficiency loss for different busbar width when structuring the front TCO; assuming a front junction bottom cell with (green) and without (red) intermediate layer structuring, and with (solid line) and without (dashed line) edge recombination.*

Notably, front side TCO structuring is complicated by the presence of the surrounding busbar, which is usually not part of the active cell area in such small devices (see **Figure 1**). The metal busbar itself is very conductive and likely makes good contact to the underlying ETL, and thus limits the TCO structuring geometry to the busbar geometry. In **Figure 5** it can be seen that the busbar width should be kept below ~1 mm in the case of front TCO structuring to keep the related perimeter efficiency loss moderately low. The busbar influence is independent of the intermediate layer conductances, and only little less for the case of no edge recombination. Notably, the trends in **Figure 5** are to good approximation independent of the junction location in the bottom cell, and are therefore applicable also to e.g. a fully structured rear-junction design.

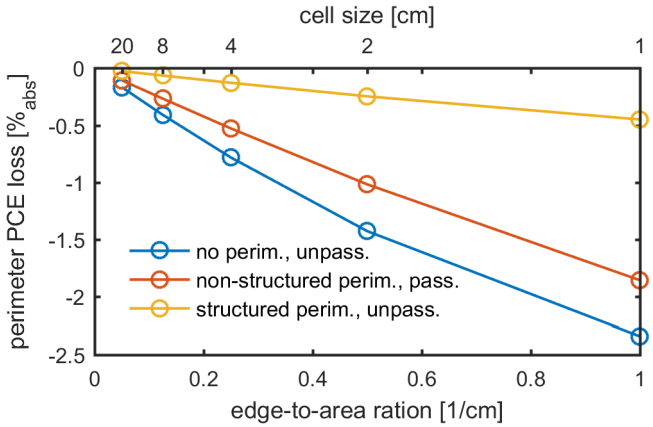

Figure 6. *Perimeter efficiency loss for varying active cell size, for 3 different cases: i) no perimeter, unpassivated edge, representing a same-size cut-out top and bottom cell; ii) non-structured perimeter with a passivated edge; iii) well-structured perimeter with an unpassivated edge.*

In **Figure 6** simulation results with varying cell sizes and different perimeter configurations are shown. It can be seen that the losses scale well with the edge-to-area ration of the active cell. It can further be seen that effort of creating a dark perimeter with edge passivation and doing a masked measurement has only little benefit over simply cutting the full tandem cell and doing a full-area illumination measurement. Also it is observed that the latter approach results in significantly less efficiency loss compared to an unstructured dark perimeter with an unpassivated edge (3-4 $\%_{abs}$ efficiency loss for 1 cm cell size, see **Figure 4**). This can be explained by the edge loss not being transport limited, so the dark perimeter results in a recombination loss additional to the edge recombination. Finally it can be seen in **Figure 6** that very small edge losses without perimeter structuring effort can only be expected for full wafer size tandem cells, which is in particular true as for non-cut full cells the edges are much less recombination active.

Of interest is also the dependence on the perimeter width. For a well-structured design where the silicon wafer conductance dominates the perimeter losses, the perimeter width must be larger than the minority carrier diffusion length. This is well fulfilled by few millimeter perimeter width. For other variants, the optimum width strongly depends on the concrete perimeter design and other cell properties.

Finally it is emphasized that the absolute values of efficiency losses presented in this paper are valid for the particular chosen cell properties only. While the general trends, effect magnitudes and conclusions are expected to be well transferable to other cell properties, such simulations should be repeated for a particular cell design if accurate predictions of the perimeter losses are desired.

3. Conclusions

Our simulations confirm that the dark perimeter on laboratory small-area perovskite-silicon tandem cells using a larger bottom cell can lead to substantial efficiency loss. For a common 1 cm^2 top cell placed on a larger cut-out bottom cell, the efficiency loss is around 4 $\%_{abs}$, dominated by bottom cell edge recombination, if no measures are taken for its suppression. We clarify that the perimeter loss can be reduced by decreasing lateral conductance of either electrons or holes, both in the top and bottom cell, respectively. This is complicated by the fact that in a tandem cell, carriers in one sub cell can be laterally transported as the opposite carrier type in the other sub cell by crossing the tunneling or recombination junction. In particular the unavoidable significant lateral conductance of the silicon wafer both for majority but also for minority carriers must therefore be considered to counteract loss suppression when reducing lateral conductance of layers between the sub cells, like the recombination TCO layer. We investigate the potential of perimeter loss suppression via structuring the top, bottom and intermediate conductive layers, which means removing their lateral (or vertical) conductance in the perimeter region. It is emphasized that a conductive bottom cell emitter ($R_{sheet} \leq 10^3$ Ω/□) in the dark perimeter must strictly be avoided, which is fulfilled in SHJ cells but not necessarily in other cell concepts. Three options requiring only a single layer structuring are identified to reduce perimeter losses to ~0.5 $\%_{abs}$: a) using a rear-junction bottom cell and structuring the rear side emitter and metallization only, b) structuring the intermediate conductive layer in a front-junction bottom cell, however with the main effect of achieving a very high (> 10^4 Ωcm^2) contact resistivity between the sub cells in the perimeter, and c) structuring the front side TCO only for a front-junction bottom cell, ensuring also high R_{sheet} of all intermediate layers (> 10^3 Ω/□) or negligible edge recombination. For the latter approach the busbar width must be small (< 1mm), as the busbar outside of the illuminated area provides parasitic lateral conductance at the front, basically increasing the unstructured front TCO area. We also find that the unavoidable conductance of the silicon wafer results in a ~0.2 $\%_{abs}$ lower limit for the perimeter loss, which is also present in record devices with high structuring effort. As expected, the perimeter losses are reduced when manufacturing larger cells, as they scale with the edge-to-area ratio of the active cell size.

Data availability statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Author contributions

A. Fell: Conceptualization, Methodology, Software, Investigation, Writing – Original Draft; **M. Bivour**: Conceptualization, Methodology, Investigation, Writing – Review & Editing, Project administration; **M. Hanser**: Methodology, Investigation, Writing – Review & Editing; **M. Schubert**: Writing – Review & Editing, Funding acquisition.

Competing interests

The authors declare no competing interests.

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