

# Reduction of Scarce Materials in Silicon Heterojunction Solar Cells and Implications on the Performance in the Field

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**Abstract.** In the first part of this work the potential to save silver for n-type silicon heterojunction solar cells was investigated. Cells were produced with varied frontside screen opening (30-50  $\mu\text{m}$ ). The groups were compared for efficiency at different irradiation levels and frontside silver laydown. For five busbar configuration large opening with low series resistance led to the highest efficiency for high irradiation around 1000  $\text{W}/\text{m}^2$  while for low irradianations all cells performed similarly. For busbarless cells lower silver laydown led to similar efficiency with slight advances for narrow screen opening. In summary cell technologies with small busbar-pitch are more tolerant for low-silver metallization. In the second part the impact of the transparent conductive oxide (TCO) was addressed. Silicon Heterojunction cells were produced with either ITO (indium tin oxide) only or an ITO-AZO-ITO (aluminium doped zinc oxide) stack, enabling an ITO reduction of about 50%, leading to a tolerable efficiency-drop of 0.3%. These internal samples were compared to industrial heterojunction-precursors (post ITO) with reference and low silver consumption frontside metallization. For both parts IV measurement showed that series resistance has a strong impact on efficiency but a rather small impact on low light-efficiency. Considering low light conditions TCO-precursor type with differences in passivation have a strong impact. On module level similar irradiation dependence of the efficiency was found and in temperature-dependent IV-measurements a positive impact of high-quality passivation on the temperature coefficients was found while an increase of the series resistance had a negative impact on the temperature dependence.

**Keywords:** Heterojunction, Field Performance, Silver Consumption, Indium Consumption

## 1. Introduction

In the coming years solar cells with selective passivating contacts, like Tunnel Oxide Passivating Contacts (TOPCon) and Silicon Heterojunction (SHJ), will show a strong increase in market share, according to ITRPV roadmap [1], and due to the overall growth of the PV industry huge production capacities for these technologies are expected to be installed. In comparison to TOPCon, SHJ has the highest efficiency ( $\eta$ ) potential among the Si-based single junction cells and the highest  $\eta$  are achieved on cell 26.81% and module level 23.89% [2], [3]. But for large scale cell and module production there are some challenges for SHJ due to the significant consumption of scarce materials, especially silver (Ag), Indium (In) and Bismuth (Bi) [4], [5]. Here In is used for the deposition of the transparent conductive oxide (TCO) layer in form of

indium tin oxide (ITO) on top of the amorphous silicon passivation layers. And Ag as noble metal with high conductivity and chemical inertness is typically the basis of low temperature paste (LTP) that is applied for front- (FS) and rear-side (RS) SHJ metallization. For module integration at low temperature Bi-containing solder is sometimes applied due to the lower melting temperature and the potential to reduce the thermal budget during interconnection. In this work we focus on In- and Ag-consumption on cell level but also discuss the impact on both, cell and module considering implications for low light behaviour. Further for modules also the temperature dependence is studied.

## 2. Experimental

Two experiments were conducted to show the effect of reducing the consumption of scarce materials in a SHJ production. The first experiment focused on the impact of Ag LTP laydown on busbarless (0BB) and five busbar (5BB) solar cells. While the second part deals with the partial substitution of ITO by a stack of aluminium doped zinc oxide (AZO) + ITO and additionally differences on SHJ precursor level between internal and external industrial ITO samples. These are analysed on cell and module level under standard testing conditions (STC) but also for varied irradiation and temperature.

### 2.1 First Experiment: Variation of Finger Width and Paste Laydown

In the first experiment the impact of LTP laydown on the FS metallization of SHJ cells based on industrial ITO precursors (M2+, n-type Cz wafer, after a-Si and ITO deposition) is studied by varying the nominal finger width  $w_N$  from 30, 35 and 40  $\mu\text{m}$  for a fixed metallization layout with a finger pitch of 1.96 mm and a separate continuous BB print (dual print) as well as an additional 50 $\mu\text{m}$  layout with 1.46 mm finger pitch including segmented busbars (reduced shading compared to continuous BB). The cell  $\eta$  is studied irradiation dependent [6] for 0BB and 5BB cells where lateral finger line resistance  $R_{\text{LINE}}$  is almost negligible for 0BB but leads to substantial losses for 5BB due to the large busbar pitch [7], [8].

### 2.2 Second Experiment: Variation of PVD Precursor and Metallization

In the second experiment the partial substitution of ITO by AZO is investigated. Due to the chemical instability of AZO and issues with high contact resistance to neighbouring metal or passivation layers the AZO is combined with ITO in an ITO-AZO-ITO stack [9], [10], [11]. Compared to pure ITO films with the same nominal thickness (105nm on planar) the ITO consumption is reduced by ~50% or more on FS and RS. This ITO-AZO-ITO stack (group 2) is compared to pure ITO references (group 1) that were also processed internally. The metallization in chosen conservative for the 5BB cells with optimal efficiency at STC for  $w_N = 40 \mu\text{m}$  combined with a new generation LTP, leading to +0.1%  $\eta$  compared to the first experiment for the same  $w_N$ . The same metallization was applied also to industrial ITO precursors (iITO, same type as in first experiment, group 3). In another group (4) the industrial substrate is metallized with a different LTP with in comparison high bulk resistivity and low laydown on the FS. The chosen layout exhibits also a pitch of ~ 2 mm but finger width and LTP laydown were significantly reduced. The cells were characterized (IV STC and low light) and cells for module integration were selected. Six cells per group were integrated into glass-backsheet modules after conventional soldering as interconnection technique (module area 1980cm<sup>2</sup>, ~ 25% inactive area). The modules were finally compared by electroluminescence (EL) images as well as temperature- and irradiation-dependent IV measurements. The whole process sequence is shown in Fig. 1.

Precursor origin / TCO	ISE ITO	ISE ITO-AZO-ITO	Industry iITO	Industry iITO
RS metal	Low- $\rho$ LT-paste: 237 fingers / pitch 0.65 mm, $w_N = 40\mu\text{m}$			
FS metal	80F / pitch 2.0 mm			
	Low- $\rho$ LT-paste		High- $\rho$ LT-paste	
	$w_N = 40\mu\text{m} \sim 50\text{mg Ag}$		$w_N = 24\mu\text{m} \sim 30\text{mg}$	
Cells	IV characterization, selection of best cells			
Modules	Module integration (IR soldering 5BB, std. ribbon, ...)			
	EL, IV (STC, low light and TC)			

Figure 1. Process flow of second experiment 2 with varied TCO and FS metallization.

### 3. Results

#### 3.1 First Experiment: Variation of Finger Width and Paste Laydown

The different groups were metallized with varied finger width ( $w_N = 30\text{-}50\ \mu\text{m}$ ) by dual print, for  $50\ \mu\text{m}$  a different layout and single print process was applied. The results for layout variations are summarized in Tab 1. Comparing  $30\ \mu\text{m}$  and  $40\ \mu\text{m}$  the wet laydown for the grid fingers was reduced by almost 50% for  $30\ \mu\text{m}$ , but the maximal STC- $\eta$  drops with 0.5% substantially for 5BB cells (Fig. 2 (b)). Here the increased  $R_{\text{LINE}}$  leads to series resistance ( $R_s$ ) related losses for finer grid lines. Looking at the 0BB measurements (Fig. 2 (a)) the impact of laydown on  $\eta$  is negligible, all groups show median  $\eta$  in the range 22.3-22.4%, the impact of  $R_{\text{LINE}}$  is neglected in the 0BB measurement and the rather small variations might have another root cause e.g., wire contact homogeneity in IV measurement. The large difference between 0BB and 5BB measurement is highlighted by the value  $\Delta(\eta_{0\text{BB-}5\text{BB}}^{\text{STC}})$  that describes the  $\eta$  loss when 0BB is converted to 5BB. The last two columns in Tab. 1 display the maximum  $\eta$  found in the irradiance dependent 5BB measurements, also the irradiation level is documented. From low to high paste laydown the maximum found  $\eta$  increases and the optimum shifts from smaller to higher irradiation. This result is also visualized in Fig. 2 where the irradiation dependent  $\eta$  is displayed for 0BB and 5BB configuration. 0BB not limited by  $R_{\text{LINE}}$  shows increasing  $\eta$  for higher irradiation not dependent on the laydown. While for 5BB the  $\eta$  for low irradiation is similar for all groups but for higher irradiation the groups are split depending on the paste laydown /  $R_{\text{LINE}}$ . This result shows the importance of reducing the wire or busbar pitch to achieve higher  $\eta$  while reducing the Ag consumption.

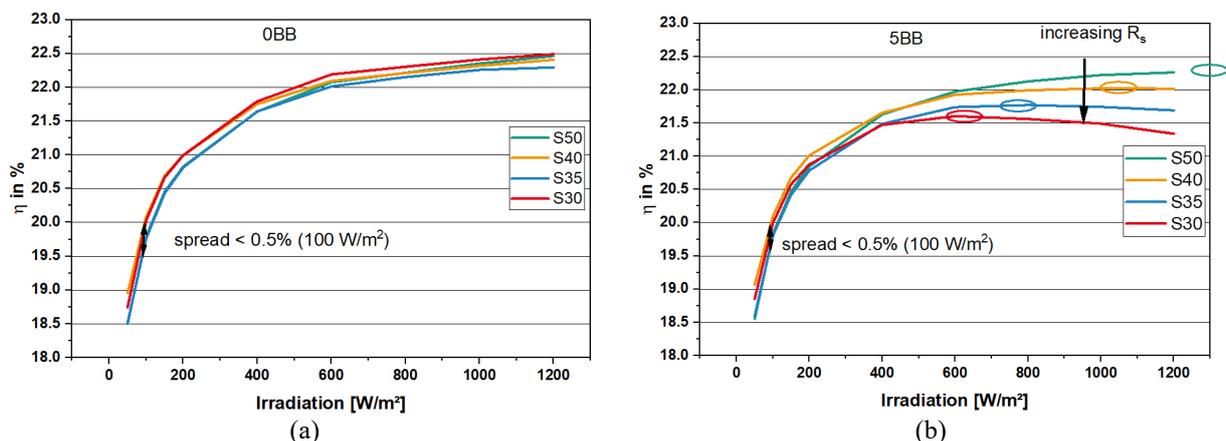


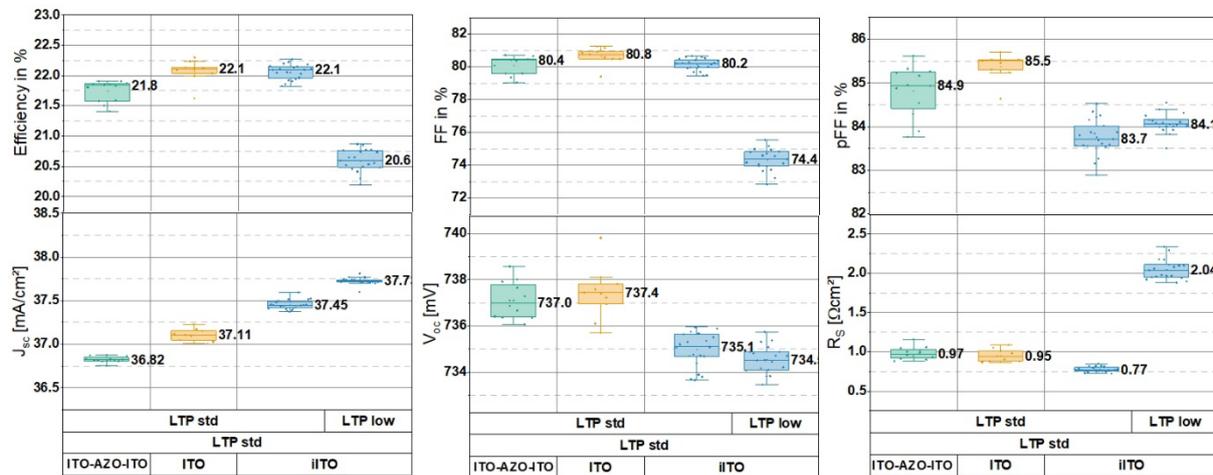
Figure 2. Efficiency versus irradiation in (a) 0BB and (b) 5BB configuration.

**Table 1.** FS-finger laydown and (median)  $\eta$  for 0BB and 5BB with varied finger width. In the last to columns the peak  $\eta$  per group in the irradiance dependent measurements (see Fig. 2(b)) are shown, the corresponding irradiance is also documented.

$W_N$	Finger pitch	Layout	Laydown	$\eta_{0BB\ STC}$	$\eta_{5BB\ STC}$	$\Delta(\eta_{0BB-5BB\ STC})$	Irradiation at $\eta_{5BB\ peak}$	$\eta_{5BB\ peak}$
[ $\mu m$ ]	[mm]		[mg]	in %	in %	in %	[ $W/m^2$ ]	in %
30	1.96	finger only	29	22.4	21.5	0.9	600	21.6
35	1.96	finger only	43	22.3	21.7	0.5	800	21.8
40	1.96	finger only	55	22.3	22.0	0.3	1000	22.0
50	1.56	finger + BB	96	22.4	22.2	0.1	$\geq 1200$	22.3

### 3.2 Second Experiment: Variation of PVD Precursor and Metallization

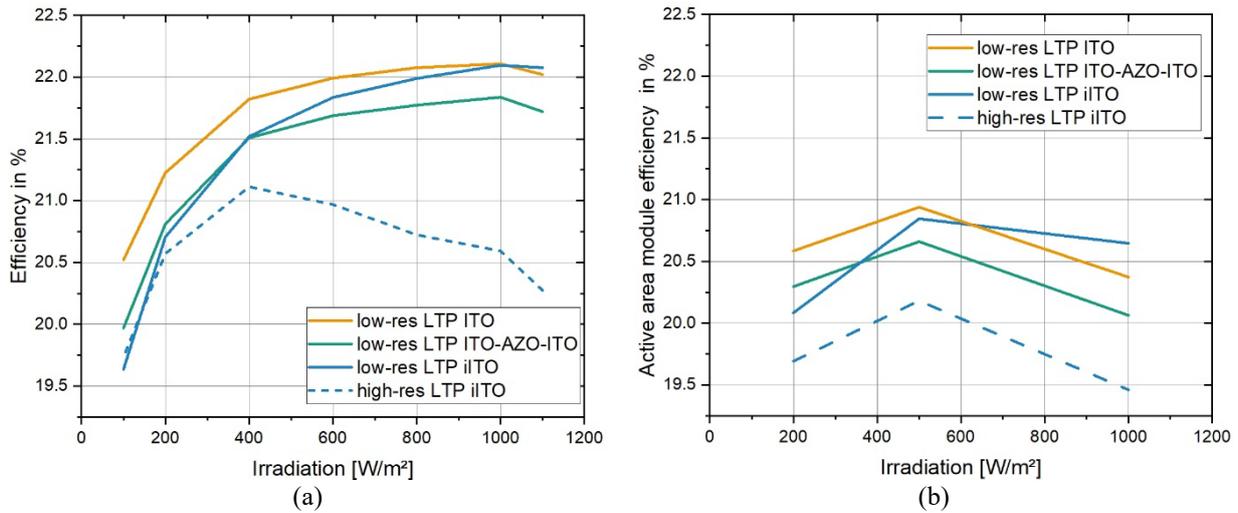
In the second experiment the effect of TCO and precursor type is studied. The experiment overview is shown in Fig. 1. After metallization and curing the 5BB cells were characterized at the cell tester, Fig. 3 shows the IV data. The cells with both side ITO-AZO-ITO stack show an  $\eta$  reduction of 0.3% compared to the ITO reference, roughly two third originate from lower short circuit density ( $J_{sc}$ ) while one third is coming from lower fill factor (FF). Open circuit voltage ( $V_{oc}$ ) is reduced only slightly. The lower pseudo fill factor (pFF) indicates a loss in passivation quality at maximum power point,  $R_s$  is on the same level, compare [11]. The industrial ITO (iITO) samples show the same  $\eta$  of 22.1% compared to the internal ITO samples but differences in the IV parameters were found. The iITO samples show higher  $J_{sc}$  and lower  $R_s$ , but these advantages are compensated by poorer passivation ( $V_{oc}$ , pFF) that result in an overall lower FF. For the last group the metallization on the FS is adapted for low Ag consumption, similar as in the prior experiment this results in lower  $\eta$  due low FF driven by a high  $R_s$ .  $J_{sc}$  is improved for the low laydown group due to the reduced shading of the narrower fingers.



**Figure 3.** IV results on cell level for varied TCO / precursor type and metallization.

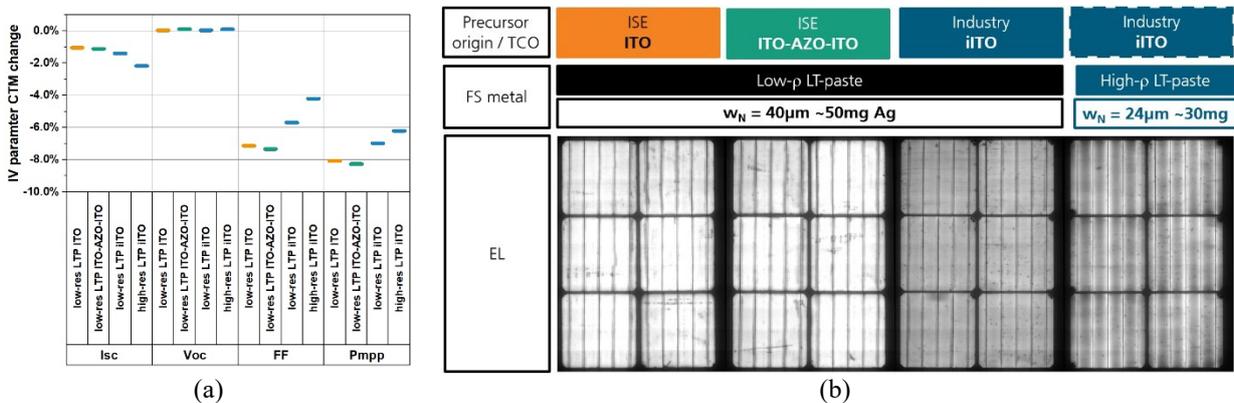
Further IV curves were recorded at varying irradiation conditions to study the impact of the SHJ precursor and metallization variations also under low light conditions. Results on cell level are shown in Fig. 4 (a). The effect of high  $R_s$  is again clearly visible and here even more pronounced as in the first experiment. Pure ITO and ITO-AZO-ITO show a similar trend, the curve is shifted by  $\sim 0.3\%$   $\eta$  as discussed for STC parameters above. Comparing external iITO and internal ITO STC  $\eta$  is similar in both cases. At 1100  $W/m^2$  iITO performs better due to the lower  $R_s$ . When the irradiation is reduced below STC the ITO samples outperform the iITO samples due to improved passivation (pFF,  $V_{oc}$ ) and decreasing impact of  $R_s$ . For 200  $W/m^2$

and lower irradiation the ITO-AZO-ITO samples show higher  $\eta$  compared to iITO, also here due to the improved passivation properties.



**Figure 4.** Efficiency as a function of varied irradiation for 5BB cells on (a) cell level and (b) after module integration.

Six 5BB full cells from each group were selected and integrated into modules and then characterized at Fraunhofer ISE Callab. In Fig. 4 (b) the irradiance dependence of the module  $\eta$  (based on the active cell area due to  $\sim 25\%$  inactive module area) is shown. Overall, the  $\eta$  level is substantially decreased due to Cell to Module (CTM) losses, that are summarized in Fig. 5 (a). For the modules non-AR coated float glass was used what lead to a  $J_{sc}$  reduction by 1-2%, iITO suffers from slightly higher optical losses compared to internal samples and for the narrow fingers in combination with iITO the loss is even higher, potentially due to lower amount of reflected light on the narrower fingers that is available for module internal total reflection.  $V_{oc}$  is fully transferred from cell to module, while the FF degrades by 4-7%. The largest portion of this loss is attributed to  $R_s$  related losses due to ribbon resistance and module periphery, but losses  $>4\%$  were not expected. This higher FF loss is found only for the low resistivity paste and more pronounced for the internal precursors. Here in EL, see Fig. 5 (b), a pronounced degradation next to the busbar was found, that is not visible for iITO in combination with the high resistivity paste. Compared to group 4 the groups with low resistivity LTP showed substantial degradation for iITO (2% higher  $CTM_{FF}$  loss), but even more pronounced for internal ITO and ITO-AZO-ITO (3% higher  $CTM_{FF}$  loss). We expect the reason for the reduced signal in EL is a contact resistance degradation during the soldering process where flux is applied to the busbar area and potentially interacts with the TCO-metal contact. Taking all losses into account a power degradation of 6-8% was found.



**Figure 5.** (a) Cell to Module related IV parameter losses and (b) EL images of the four modules.

Finally, the four modules were also IV characterized at varying temperatures to identify potentially differences in temperature coefficients (TC). For the different temperature IV parameters were extracted and the TCs were extracted by linear regression. The results are summarized in Tab. 2. For all samples similar TCs for  $J_{sc}$  and  $V_{oc}$  were found, while  $TC_{FF}$  and subsequently  $TC_{\eta}$  varied. The cell  $R_S$  increase from about  $0.8 \Omega\text{cm}^2$  (group 3) to  $2.0 \Omega\text{cm}^2$  (group 4) for iITO leads to higher temperature related FF loss (-0.03%). The improved passivation of the internal samples overcompensates the slightly higher  $R_S$  and in sum leads to a lower temperature related FF loss (-0.02%) compared to iITO with reference metallization. These result shows that reducing the paste laydown decreases not only the STC  $\eta$  but also additional  $\eta$ -reduction at higher operating module temperatures. The internal samples with high  $V_{oc}$  and pFF had the best  $TC_{\eta} > -0.3\%$ , where interestingly the TC of the FF is more prominently affected compared to the  $V_{oc}$ .

**Table 2.** Temperature coefficients extracted for the modules.

Module	$TC_{J_{sc}}$ in %	$TC_{V_{oc}}$ in %	$TC_{FF}$ in %	$TC_{\eta}$ in %
Low-res LTP ITO	0.03	-0.24	-0.08	-0.29
Low-res LTP ITO-AZO-ITO	0.03	-0.24	-0.08	-0.29
Low-res LTP iITO	0.03	-0.24	-0.10	-0.32
High-res LTP iITO	0.03	-0.24	-0.13	-0.34

#### 4. Summary, Conclusion and Outlook

Within the two experiments it was shown, that for large wire or busbar pitch, valid for 5BB, the achieved  $\eta$  around STC conditions is sensitive for reduced Ag-LTP laydown. Both increasing the laydown and/or increasing the number of printed fingers and thereby reducing the finger pitch leads to an  $\eta$ -increase. In the middle irradiation range the difference in  $\eta$  is reduced for varied laydown and disappears below  $300 \text{ W/m}^2$ . In contrast if a cell is measured (or integrated into a module) with small wire pitch the impact of the LTP laydown is drastically reduced and narrow printed fingers might be advantageous. For the extreme case of measuring 0BB cell with a wire contact no impact of the laydown was found. The small  $\eta$  differences likely originate from narrower fingers and / or contacting issues. In summary cell or module technologies with small collecting electrode pitch allow significant Ag laydown reduction. Also, optimization of the metallization design for a certain irradiance level (e.g. for BIPV) allows significant Ag savings. In the second part of the investigation encouraging results for 50% substitution of ITO by AZO were found with a difference in  $\eta$  of  $\sim 0.3\%$ . Integration into modules was also successful. A degradation especially of the internal samples during interconnection was found but for both ITO and ITO-AZO-ITO stacks. In the same experiment additionally the impact of passivation quality and  $R_S$  on the irradiance and temperature dependence were studied on module level. Improving the passivation quality (pFF,  $V_{oc}$ ) leads to advantages in both STC and more pronounced for low light  $\eta$ . Also, for the temperature dependence a high passivation level leads to less  $\eta$  loss due to increased temperature. Here decreasing the Ag laydown and thereby increasing the cell  $R_S$  leads to a more pronounced temperature dependence of the  $\eta$  ( $TC_{FF}$ ).

In upcoming experiments, it is planned to investigate the optimal grid layout with narrow  $w_N$  and reduced LTP laydown for smaller BB/wire pitch cell layout also for larger wafer formats. Finally, the applicability of Ag/Cu or Cu pastes for SHJ will be addressed.

#### Data availability statement

The data supporting the results of this contribution are available upon reasonable request from the corresponding author

## Author contributions

Sebastian Pingel: Conceptualization, Data curation, Investigation, Visualization, Writing

Anamaria Steinmetz: Conceptualization, Investigation, Writing, Funding acquisition, Review & Editing

Martin Bivour: Supervision, Funding acquisition, Review

Ioan Voicu Vulcanean, Timo Wenzel, Philipp Schmid, Henning Nagel, Winfried Wolke, Vasileios Georgiou-Sarlikiotis, Ulli Kräling: Investigation

## Competing interests

The authors declare no competing interests.

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## References

1. International Technology Roadmap for Photovoltaic (ITRPV) Report (2022)
2. LONGi, "At 26.81%, LONGi sets a new world record efficiency for silicon solar cells". <https://www.longi.com/en/news/propelling-the-transformation/> (21.04.2023 accessed)
3. A. Bhambhani. "Germany's TUV SUD Confirms Risen Energy Claim Of Achieving 23.89% Efficiency For Heterojunction Modules With 741W+ Output" <https://taiyang-news.info/technology/risen-energy-hits-23-89-efficiency-for-hjt-modules/> (21.04.2023 accessed)
4. B. Hallam et al., "Challenges and Opportunities for Terawatt-Scale Deployment of n-Type Solar Cell Technology" SiliconPV, 2022, not published (yet)
5. E. Gervais et al., "Sustainability strategies for PV: framework, status and needs", EPJ Photovoltaics, 2021, DOI: 10.1051/epjpv/2021005
6. G. Deboutte, PV Magazine, "CEA-INES reduces silver consumption in M2 heterojunction solar cell". <https://www.pv-magazine.com/2022/10/26/cea-ines-reduces-silver-consumption-in-m2-heterojunction-solar-cell/> (21.04.2023 accessed)
7. B. Litzenburger et al., „Low Light performance of Solar Cells and Modules“, EU PVSEC, 2014, DOI: 10.4229/EUPVSEC20142014-5CV.2.6
8. S. Pingel et al, "Low-Temperature Ag-Paste Screening for Silicon Heterojunction Solar Cells and Modules", EUPVSEC, 2020, DOI: 10.4229/EUPVSEC20202020-2DV.3.17
9. S. Janke et al. "Approaches for SHJ Cells with Low or No Indium Content", SiliconPV, 2022, not published (yet)
10. M. Dimer et al., "Potential of Sputtered AZO Layers for the Industrial Manufacturing of Hetero Junction Solar Cells", WCPEC / EU PVSEC, 2022, 10.4229/WCPEC-82022-1DO.12.4

11. P. Schmid et al., „Reducing Indium Consumption in Silicon Hetero Junction Solar Cells with TCO Stack Systems of ITO and AZO“, IEEE, 2023, will be published, DOI: 10.1109/JPHOTOV.2023.3267175